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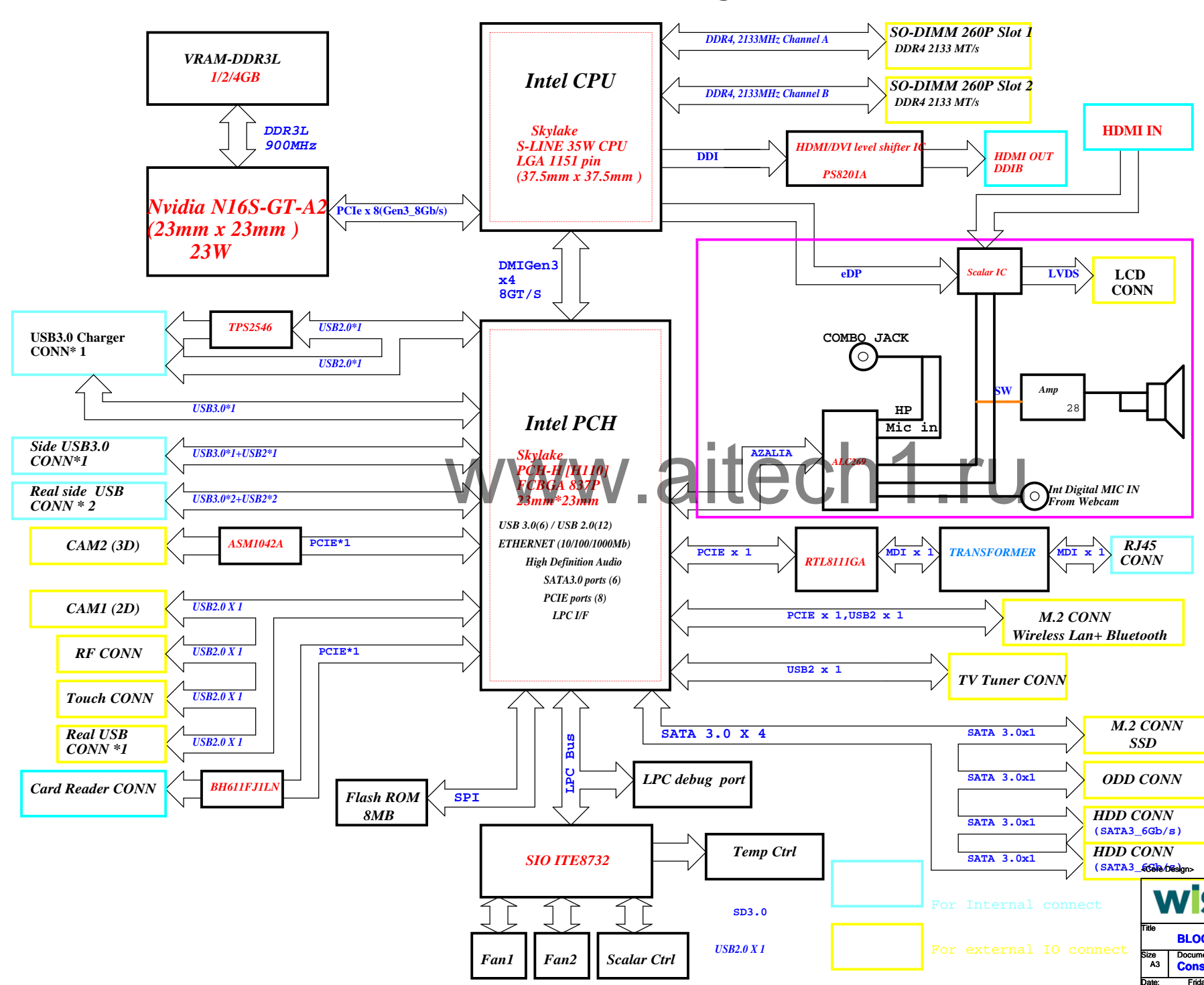
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| 77   | GPU (2/5): DIGITALOUT       |          |
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Model: AIO, Scotland  
SCH Ver: -1A  
PCB Ver:-1A  
PCB NumSAbber:15005  
PCB P/N:  
3PD03Y010001

PCB BOARD SIZE  
6 Layers  
271mmX198mm

BOM Configuration  
Unmount:(R\_)  
GPU:(G\_)  
Hynix RAM:(H\_)  
SAMSUNG RAM:(M\_)  
UMA: (U\_)  
2D WEBCAM: (W2\_)  
3D WEBCAM: (W3\_)  
XDP:(X\_)  
AMP:(A\_)  
SCALAR:(S\_)  
SCOTLAND:(L\_)  
BRISTOL:(B\_)  
USB3 TYPE C:(U3C\_)  
USB3 TYPE A:(U3A\_)

# Scotland238 Block Diagram (GPU)



| 5V/3D3V DC/DC<br>RT8243B    |  |
|-----------------------------|--|
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | 5V_AUX_S5<br>3D3V_AUX_S5<br>5V_Charger<br>3D3V_A |
| CPU/GT DC/DC<br>NCP81203    |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | VCC_CORE<br>GFX_CORE                             |
| VCCSA DC/DC<br>RT8237C      |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | VCC_SA   |
| VCCIO DC/DC<br>RT8237C      |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | VCC_IO   |
| 12V DC/DC<br>RT8115C        |  |
| INPUTS                      | OUTPUTS  |
| 3D3V_S0                     | 12V_S0   |
| MEM/MEMVTT DC/DC<br>RT8207P |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | VDDQ<br>0D6V_VREF_S0                             |
| 1D0V DC/DC<br>RT8237C       |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | 1D0V_S5  |
| VGA DC/DC<br>NCP81172       |  |
| INPUTS                      | OUTPUTS  |
| DCBATOUT                    | VGA_CORE   |

| PCB LAYER |           |
|-----------|-----------|
| L1:Top    | L5:VCC    |
| L2:GND    | L6:Bottom |
| L3:Signal |           |
| L4:Signal |           |

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|       |                         |                 |                       |
|-------|-------------------------|-----------------|-----------------------|
| Title | BLOCK DIAGRAM           |                 |                       |
| Size  | A3                      | Document Number | Consumer AIO Scotland |
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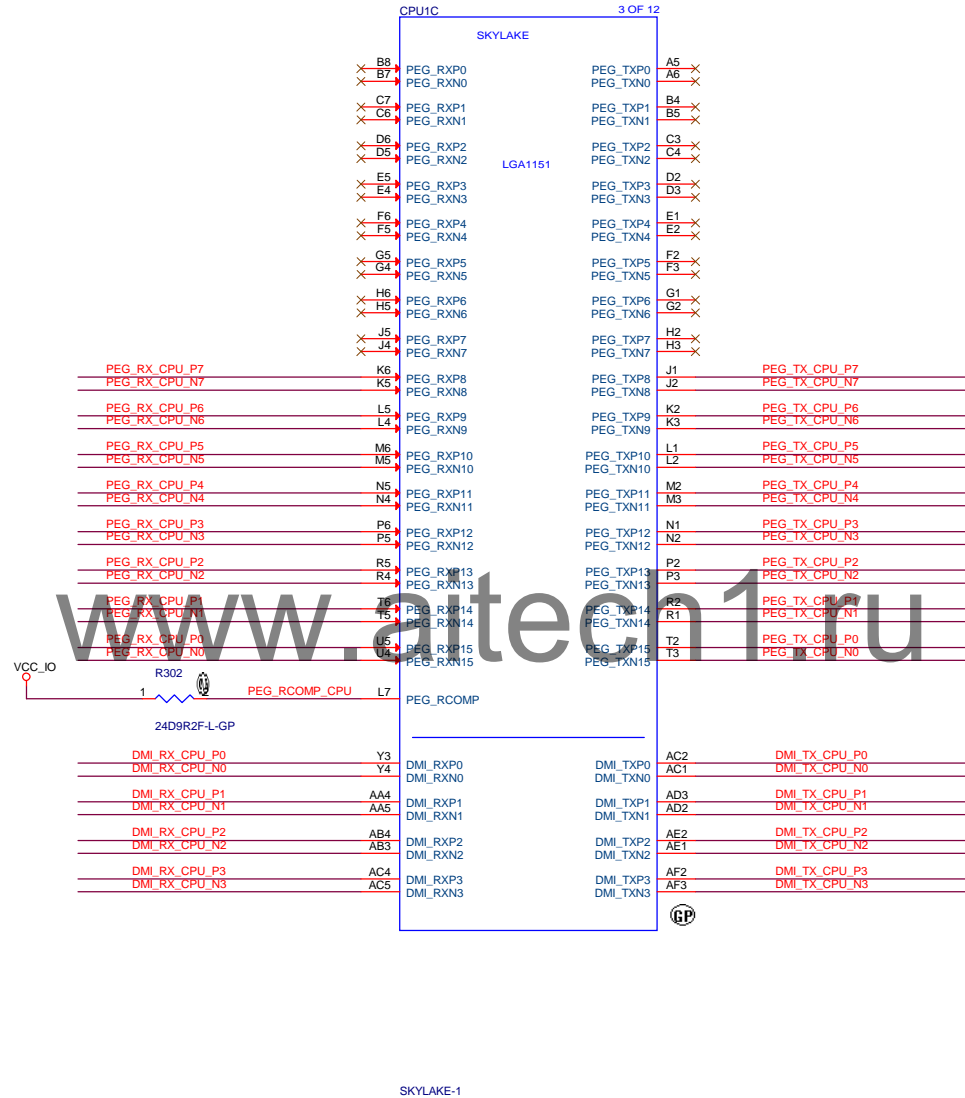
2014/8/5  
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## PEG

76 PEG\_TX\_CPU\_P[0..7] <<<<  
76 PEG\_TX\_CPU\_N[0..7] <<<<  
76 PEG\_RX\_CPU\_P[0..7] <<<<  
76 PEG\_RX\_CPU\_N[0..7] <<<<

## DMI

16 DMI\_RX\_CPU\_P[0..3] <<<<  
16 DMI\_RX\_CPU\_N[0..3] <<<<  
16 DMI\_TX\_CPU\_P[0..3] <<<<  
16 DMI\_TX\_CPU\_N[0..3] <<<<



<Core Design>

**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title  
**CPU(PCIE/DMI)**

Size Document Number  
Customer **Consumer AIO Scotland**

Rev  
SA

Date: Friday, August 21, 2015 Sheet 3 of 107

## CPU XDP

4.99 XDP\_PCUDEBUG3 >>>  
99 CFG0[0..15] >>>  
99 SKL\_PCUSTB\_0\_DP >>>  
99 SKL\_PCUSTB\_0\_DN >>>  
99 SKL\_PCUSTB\_1\_DP >>>  
99 SKL\_PCUSTB\_1\_DN >>>  
99 BPM\_CPU\_N0 >>>  
99 BPM\_CPU\_N1 >>>  
99 H\_TDO >>>  
99 H\_TDI >>>  
99 H\_TMS >>>  
20.99 H\_TCK >>>  
65.99 H\_TRST\_N >>>  
99 H\_PREQ\_N >>>  
99 H\_PRDY\_N >>>

## SVID

46 VIDSCK\_VR1 >>>  
46 VIDSOUT\_VR1 >>>  
46 VIDALERT#\_VR1 >>>

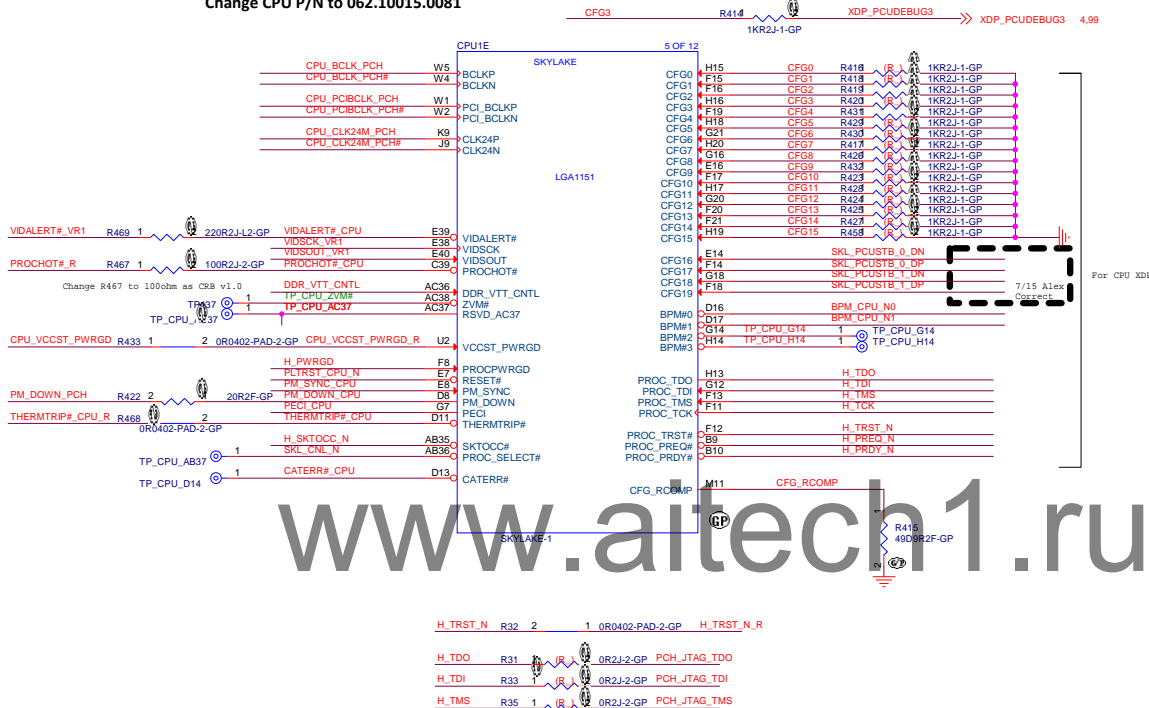
## CLOCK

18 CPU\_BCLK\_PCH >>>  
18 CPU\_BCLK\_PCH# >>>  
18 CPU\_PCBCLK\_PCH >>>  
18 CPU\_PCBCLK\_PCH# >>>  
18 CPU\_CLK24M\_PCH >>>  
18 CPU\_CLK24M\_PCH# >>>

## CONTROL

65 CPU\_VCCST\_PWRGD\_R <<<  
43.46 PROCHOT#\_R <<<  
40.50 DDR\_VTT\_CNTL <<<  
40.99 CPU\_VCCST\_PWRGD <<<  
20.65.99 H\_PWRGD <<<  
17.65.99 PLTRST\_CPU\_N <<<  
17 PM\_SYNC\_CPU <<<  
17 PM\_DOWN\_PCH <<<  
17.24 PECL\_CPU <<<  
17.79 THERMTRIP#\_CPU\_R <<<  
16 H\_SKTOCC\_N <<<  
20 PCH\_JTAG\_TDO <<<  
20 PCH\_JTAG\_TDI <<<  
20 PCH\_JTAG\_TMS <<<  
21 H\_TRST\_N\_R <<<

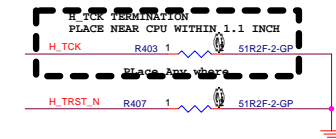
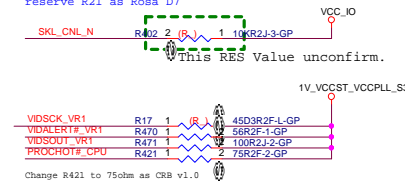
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VIDSCK  
VIDSOUT  
VIDALERT#  
Need to add Pull UP on both CPU and VR side.

| Signal    | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | W5.1 [inches] | W5.2 [inches] | R101 [Ω] | R102 [Ω] | R103 [Ω] | R104 [Ω] | VCCs [V] |
|-----------|-------------|-------------|-----------------|----------------------|---------------|---------------|----------|----------|----------|----------|----------|
| VIDSOUT   | 0.5-3       | 1-15        | 0.5-4           | 3-17                 | <0.1          | <0.1          | 100      | 100      | 0        | 10       | 1.0      |
| VIDSCK    |             |             |                 |                      |               |               | Empty    | 45       | 0        | 50       |          |
| VIDALERT# |             |             |                 |                      |               |               | 56       | Empty    | 220      | 0        |          |

2014/9/29  
reserve R21 as Rosa D7



- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation;
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express\* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express\* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express\*
  - 01 = reserved
  - 10 = 2 x8 PCI Express\*
  - 11 = 1 x16 PCI Express\*
- **CFG[7]:** PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

<Core Design>

|  |                              |   |          |
|--|------------------------------|---|----------|
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| Title<br><b>CPU (THERMAL/CLOCK/PM/CFG)</b> |                              |   |          |
| Size                                       | Document Number              | Rev   |          |
| Customer                                   | <b>Consumer AIO Scotland</b> | SA  |          |
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11 M\_A\_ACT# << >>  
11 M\_A\_ODT0 << >>  
11 M\_A\_ODT1 << >>  
  
11 M\_A\_CKE0 << >>  
11 M\_A\_CKE1 << >>  
  
11 M\_A\_CAS# << >>  
11 M\_A\_WE# << >>  
11 M\_A\_RAS# << >>  
  
11 M\_A\_ALERT# << >>  
11 M\_A\_PAR << >>

12 M\_B\_DQ[63..0]

M\_B\_DQ62  
M\_B\_DQ61  
M\_B\_DQ60  
M\_B\_DQ59  
M\_B\_DQ58  
M\_B\_DQ57  
M\_B\_DQ56  
M\_B\_DQ55  
M\_B\_DQ54  
M\_B\_DQ53  
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M\_B\_DQ1  
M\_B\_DQ0

12 M\_B\_A[13..0]

M\_B\_A13  
M\_B\_A12  
M\_B\_A11  
M\_B\_A10  
M\_B\_A9  
M\_B\_A8  
M\_B\_A7  
M\_B\_A6  
M\_B\_A5  
M\_B\_A4  
M\_B\_A3  
M\_B\_A2  
M\_B\_A1  
M\_B\_A0

12 M\_B\_DQS\_DP[7..0]

M\_B\_DQS\_DP7  
M\_B\_DQS\_DP6  
M\_B\_DQS\_DP5  
M\_B\_DQS\_DP4  
M\_B\_DQS\_DP3  
M\_B\_DQS\_DP2  
M\_B\_DQS\_DP1  
M\_B\_DQS\_DP0

12 M\_B\_DQS\_DN[7..0]

M\_B\_DQS\_DN7  
M\_B\_DQS\_DN6  
M\_B\_DQS\_DN5  
M\_B\_DQS\_DN4  
M\_B\_DQS\_DN3  
M\_B\_DQS\_DN2  
M\_B\_DQS\_DN1  
M\_B\_DQS\_DN0

12 M\_B\_BA[1..0]

12 M\_B\_BG[1..0]

12 M\_B\_CLK0

12 M\_B\_CLK1

12 M\_B\_CLK#1

12 M\_B\_CS#0

12 M\_B\_ODT0

12 M\_B\_ODT1

12 M\_B\_CKE0

12 M\_B\_CKE1

12 M\_B\_CKE2

12 M\_B\_CKE3

12 M\_B\_CKE4

12 M\_B\_CKE5

12 M\_B\_CKE6

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12 M\_B\_CKE9

12 M\_B\_CKE10

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12 M\_B\_CKE227

12 M\_B\_CKE228

12 M\_B\_CKE229

12 M\_B\_CKE230

12 M\_B\_CKE231

12 M\_B\_CKE232

12 M\_B\_CKE233

12 M\_B\_CKE234

12 M\_B\_CKE235

12 M\_B\_CKE236

12 M\_B\_CKE237

12 M\_B\_CKE238

12 M\_B\_CKE239

12 M\_B\_CKE240

12 M\_B\_CKE241

12 M\_B\_CKE242

12 M\_B\_CKE243

12 M\_B\_CKE244

12 M\_B\_CKE245

12 M\_B\_CKE246

12 M\_B\_CKE247

12 M\_B\_CKE248

12 M\_B\_CKE249

12 M\_B\_CKE250

12 M\_B\_CKE251

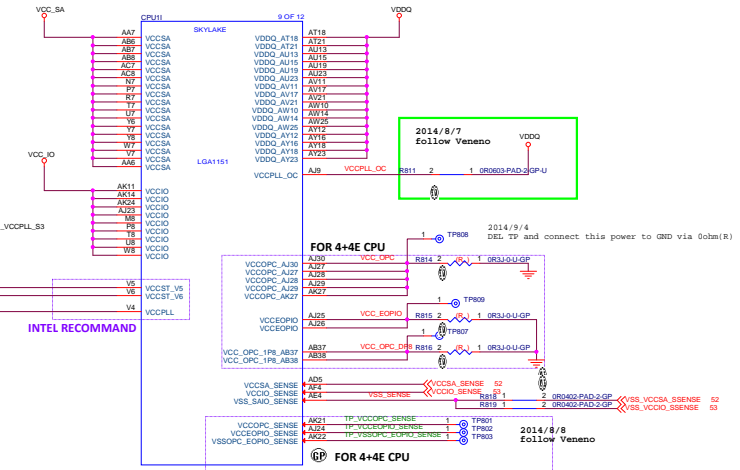
12 M\_B\_CKE252

12 M\_B\_CKE253

12 M\_B\_CKE254



Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGTG, VCCGTGTX, VCC\_OPC\_1P8, VCCOCPD and VCCOEPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.

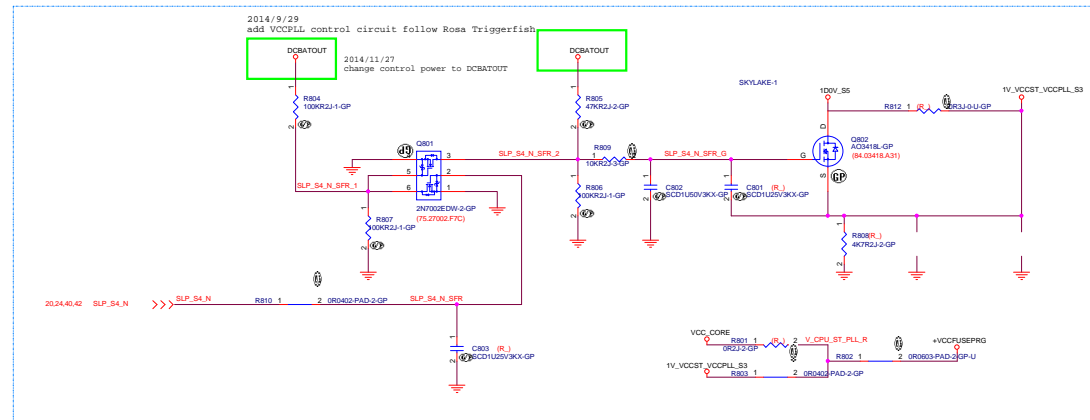
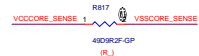


Pinout diagram for SKYLAKE-1 showing 14 pins with their functions and connections to a 1.8V supply:

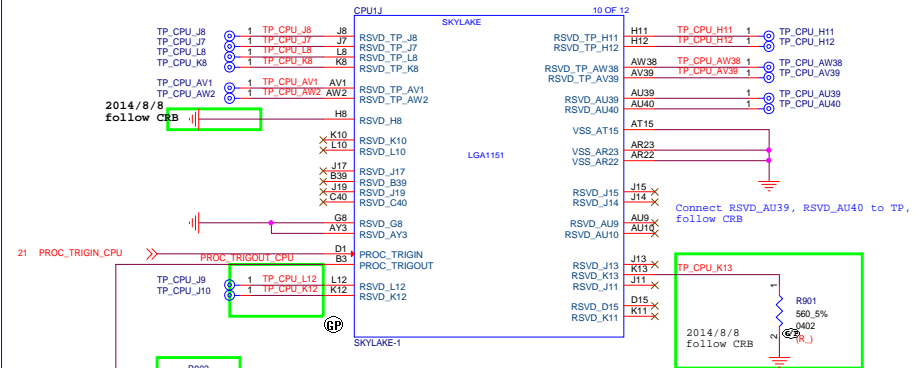
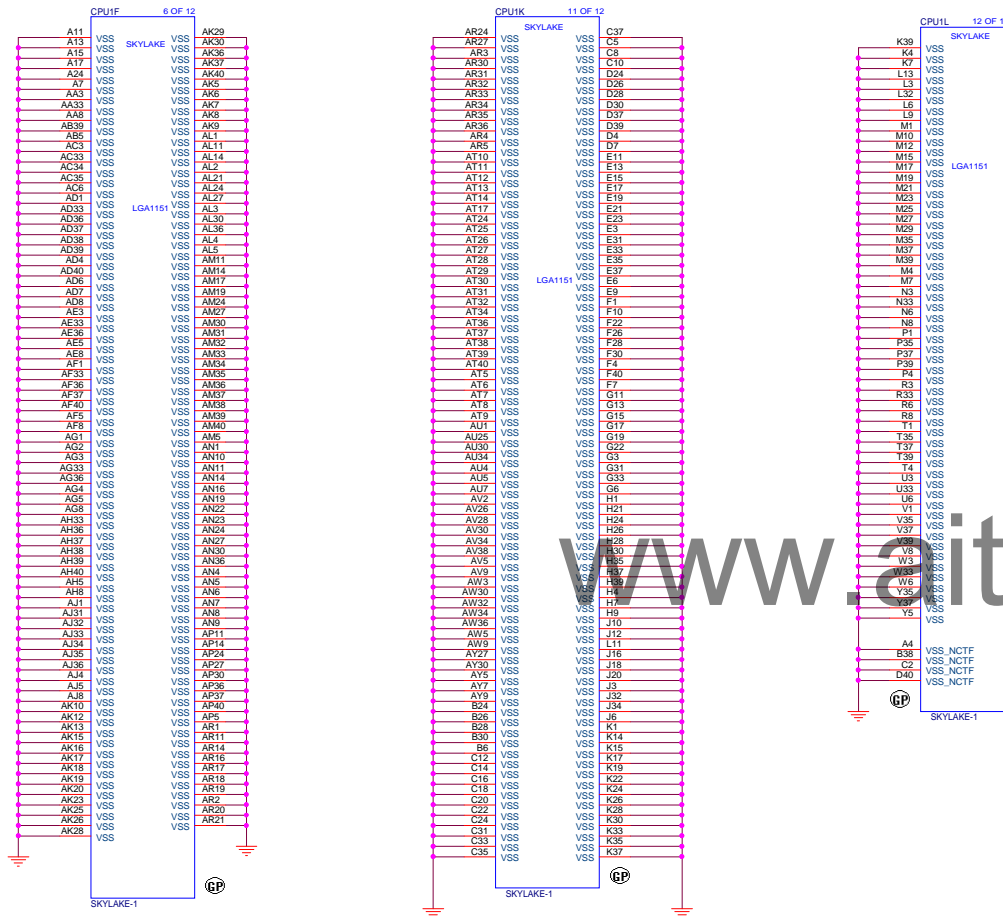
- V80: VCCGT
- W81: VCCGT
- W82: VCCGT
- W83: VCCGT
- W84: VCCGT
- W85: VCCGT
- V86: VCCGT
- V87: VCCGT
- V88: VCCGT
- V89: VCCGT
- V90: VCCGT
- V91: VCCGT
- V92: VCCGT
- V93: VCCGT

Connections to 1.8V supply:

- F30: VCCGT, DENSE
- F31: VCCGT, DENSE
- F32: VCCGT, DENSE
- F33: VCCGT, DENSE
- F34: VCCGT, DENSE
- F35: VCCGT, DENSE
- F36: VCCGT, DENSE
- F37: VCCGT, DENSE
- F38: VCCGT, DENSE
- F39: VCCGT, DENSE
- F40: VCCGT, DENSE
- F41: VCCGT, DENSE
- F42: VCCGT, DENSE
- F43: VCCGT, DENSE
- F44: VCCGT, DENSE
- F45: VCCGT, DENSE
- F46: VCCGT, DENSE
- F47: VCCGT, DENSE
- F48: VCCGT, DENSE
- F49: VCCGT, DENSE
- F50: VCCGT, DENSE
- F51: VCCGT, DENSE
- F52: VCCGT, DENSE
- F53: VCCGT, DENSE
- F54: VCCGT, DENSE
- F55: VCCGT, DENSE
- F56: VCCGT, DENSE
- F57: VCCGT, DENSE
- F58: VCCGT, DENSE
- F59: VCCGT, DENSE
- F60: VCCGT, DENSE
- F61: VCCGT, DENSE
- F62: VCCGT, DENSE
- F63: VCCGT, DENSE
- F64: VCCGT, DENSE
- F65: VCCGT, DENSE
- F66: VCCGT, DENSE
- F67: VCCGT, DENSE
- F68: VCCGT, DENSE
- F69: VCCGT, DENSE
- F70: VCCGT, DENSE
- F71: VCCGT, DENSE
- F72: VCCGT, DENSE
- F73: VCCGT, DENSE
- F74: VCCGT, DENSE
- F75: VCCGT, DENSE
- F76: VCCGT, DENSE
- F77: VCCGT, DENSE
- F78: VCCGT, DENSE
- F79: VCCGT, DENSE
- F80: VCCGT, DENSE
- F81: VCCGT, DENSE
- F82: VCCGT, DENSE
- F83: VCCGT, DENSE
- F84: VCCGT, DENSE
- F85: VCCGT, DENSE
- F86: VCCGT, DENSE
- F87: VCCGT, DENSE
- F88: VCCGT, DENSE
- F89: VCCGT, DENSE
- F90: VCCGT, DENSE
- F91: VCCGT, DENSE
- F92: VCCGT, DENSE
- F93: VCCGT, DENSE
- F94: VCCGT, DENSE
- F95: VCCGT, DENSE
- F96: VCCGT, DENSE
- F97: VCCGT, DENSE
- F98: VCCGT, DENSE
- F99: VCCGT, DENSE



2014/8/5  
Change CPU P/N to 062.10015.0081

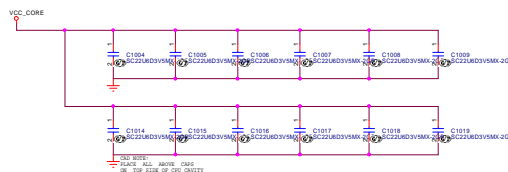
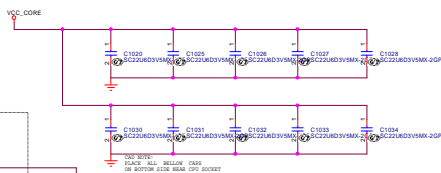


20R2J-3-GP

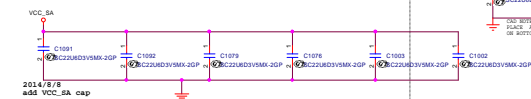
V35 VSS  
V37 VSS  
V39 VSS  
V8 VSS  
V9 VSS  
W3 VSS  
W33 VSS  
W6 VSS  
Y35 VSS  
Y37 VSS

H24 VSS  
H26 VSS  
H28 VSS  
H30 VSS  
H32 VSS  
H34 VSS  
H36 VSS  
H38 VSS  
H4 VSS  
H6 VSS  
H7 VSS

2014/8/8  
DEL VCC0PC and VCC0FIO power cap

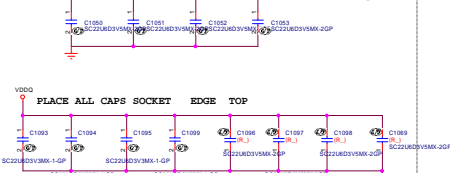


PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

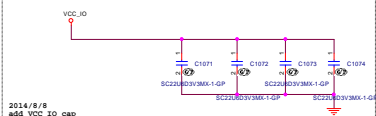


CAPS FOR DIMM

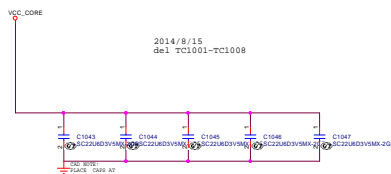
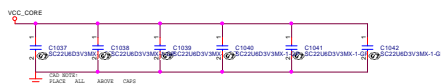
2014/8/8  
add 1.25V\_S3 cap



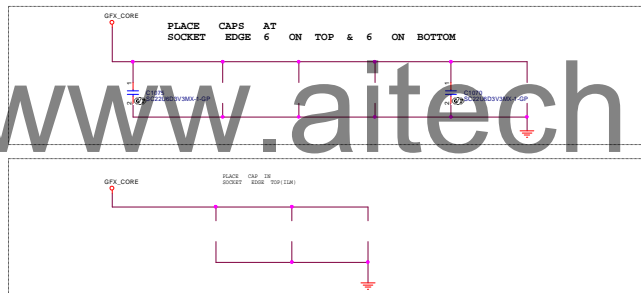
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE



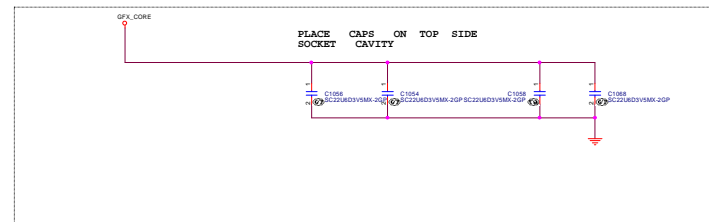
PLACE ALL CAPS OUTSIDE CPU SOCKET CAVITY ON TOPSIDE



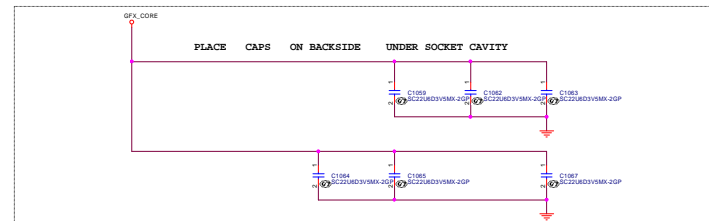
PLACE CAPS AT SOCKET EDGE 6 ON TOP & 6 ON BOTTOM



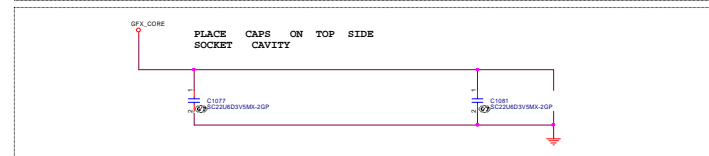
PLACE CAPS ON TOP SIDE SOCKET CAVITY



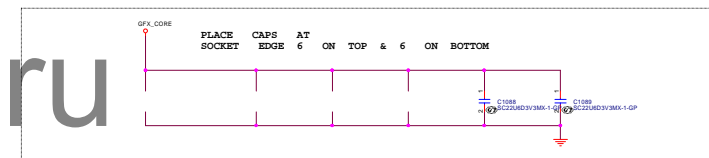
PLACE CAPS ON BACKSIDE UNDER SOCKET CAVITY



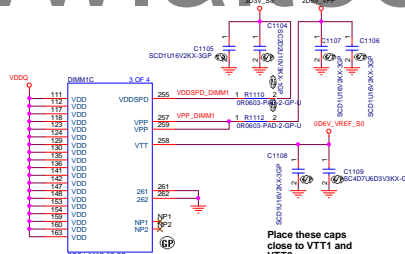
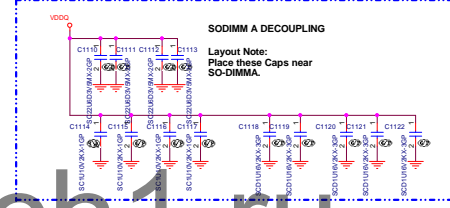
PLACE CAPS ON TOP SIDE SOCKET CAVITY



PLACE CAPS AT SOCKET EDGE 6 ON TOP & 6 ON BOTTOM



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[illegible]

Note: 0.3 ~ 7 Bit as default




Reserved

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|   |   |  |
|---|---|--|
| <Core Design>   |   |  |
|  |   | <b>Wistron Incorporated</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd<br>Hsichih, Taipei Hsien |
| Title<br><b>DDR4 DIMM_3_(R)</b>   |   |  |
| Size<br>Customer  | Document Number<br><b>Consumer AIO Scotland</b> | Rev<br>SA  |
| Date  | Friday, August 21, 2015                         | Sheet 13 of 107  |

Reserved

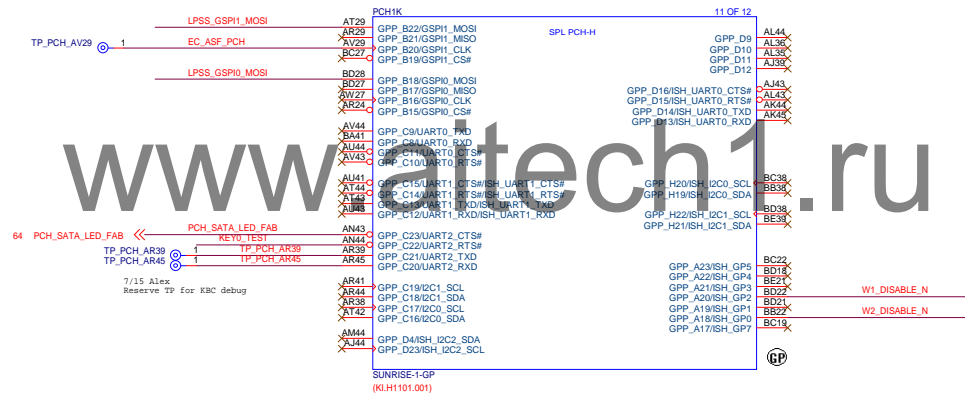
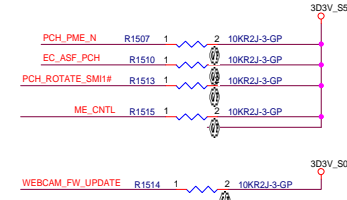
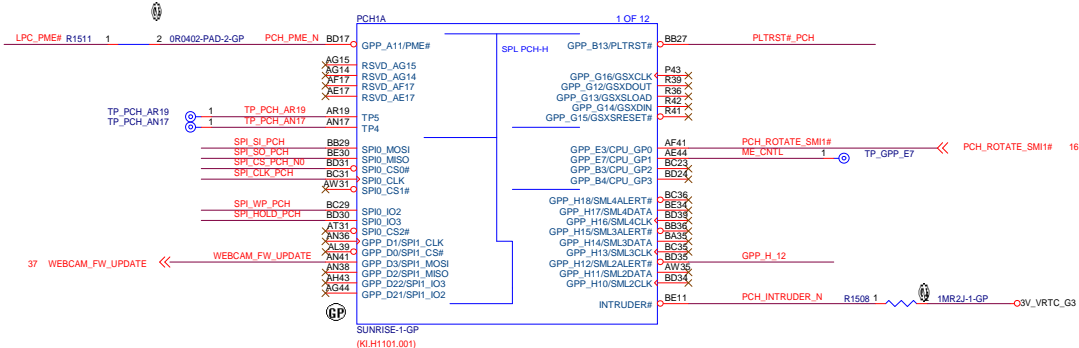
www.aitech1.ru

|   |                         |   |     |
|---|-------------------------|---|-----|
| <Core Design>   |                         |   |     |
|  |                         | <b>Wistron Incorporated</b><br>21F, 88, Sec.1 Hsin Tai Wu Rd<br>Hsichih, Taipei Hsein |     |
| Title   |                         |   |     |
| DDR4 DIMM_4_(R)   |                         |   |     |
| Size  | Document Number         |   | Rev |
| Customer  | Consumer AIO Scotland   |   | SA  |
| Date:   | Friday, August 21, 2015 | Sheet 14 of 107   |     |

24,95 LPC\_PME# >>>  
22,25,99 SPI\_SI\_PCH <<<  
22,25 SPI\_SO\_PCH <<<  
25 SPI\_CS\_PCH\_N0 <<<  
25 SPI\_CLK\_PCH <<<  
22,25 SPI\_WP\_PCH <<<  
22,25 SPI\_HOLD\_PCH <<<  
24,65,68,76,79 PLTRST#\_PCH <<<  
22 GPP\_H\_12 <<<  
20 ME\_CNTL <<<  
22 LPSS\_GSPI0\_MOSI >>>  
22 LPSS\_GSPI0\_MOSI >>>

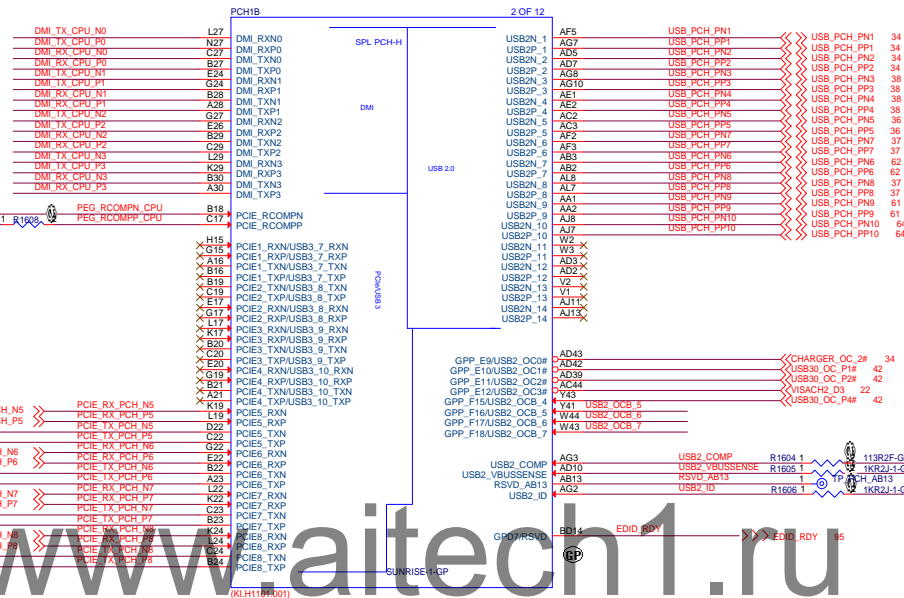
62 W1\_DISABLE\_N <<<  
62 W2\_DISABLE\_N <<<

64 KEY0\_TEST >>>



DMI

3 DMI\_TX\_CPU\_N0\_3  
3 DMI\_TX\_CPU\_P0\_3  
3 DMI\_RX\_CPU\_N0\_3  
3 DMI\_RX\_CPU\_P0\_3



## USB Table

| Pair | Device                    |
|------|---------------------------|
| 1    | USB3.0 Ext. port 1 (Side) |
| 2    | USB3.0 Ext. port 2 (Side) |
| 3    | USB3.0 Ext. port 3 (Rear) |
| 4    | USB3.0 Ext. port 4 (Rear) |
| 5    | USB2.0 Ext. port 5 (Rear) |
| 6    | TOUCH                     |
| 7    | WLAN+BT                   |
| 8    | WEB CAM (Front)           |
| 9    | TV Tuner                  |
| 10   | Wireless KB/MS receiver   |
| 11   | TBD                       |
| 12   | TBD                       |
| 13   | TBD                       |
| 14   | TBD                       |

LAN

CARD READER\_BH611FJ11N

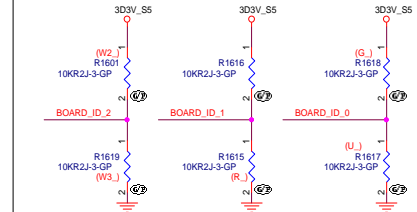
WLAN

3D Webcam ASM1042A

2014/9/9  
DD11 TO DP1  
DD12 TO DP2  
DD13 TO DP1



## BOARD ID



## SB EC Board ID Description

|     | ID2 Bit1 | ID1 Bit0 |
|-----|----------|----------|
| SA  | NA       | 0        |
| SB  | NA       | 1        |
| -1A | NA       | 0        |
| -1  | NA       | 1        |
| -2  | NA       | 0        |

|           | ID2 |
|-----------|-----|
| 2D WEBCAM | 1   |
| 3D WEBCAM | 0   |

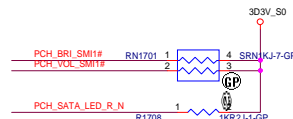
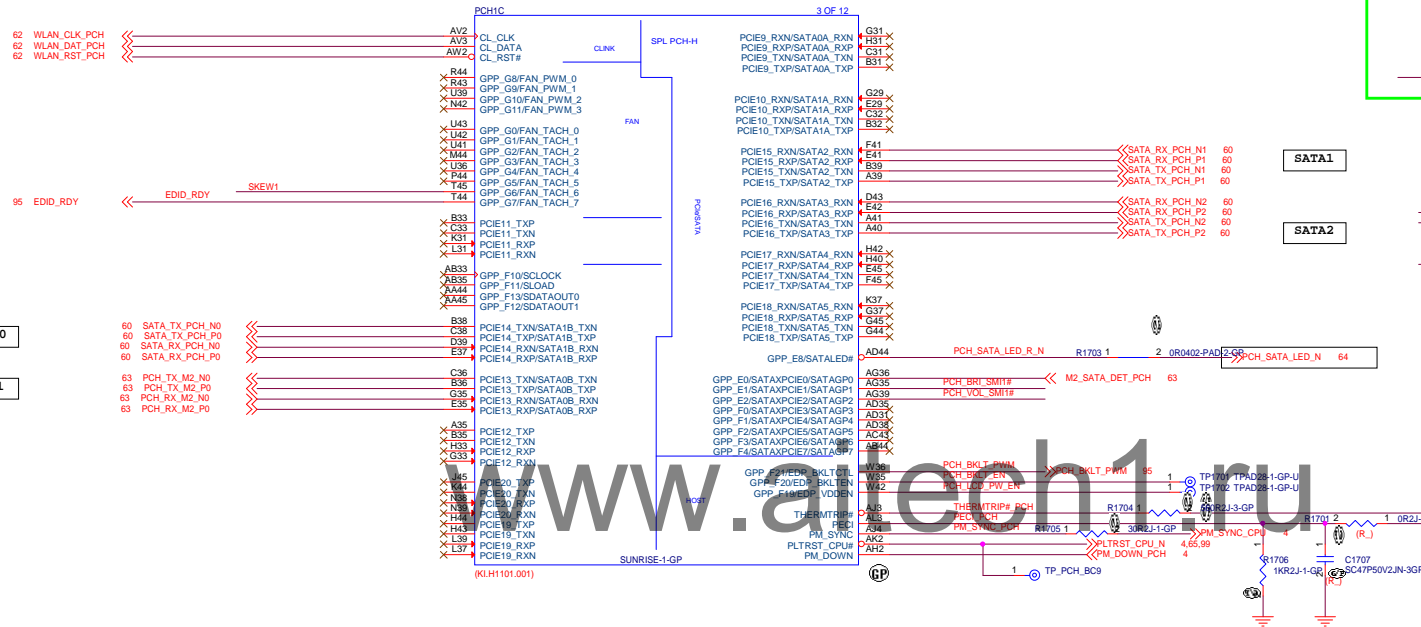
|     | ID0 |
|-----|-----|
| GPU | 1   |
| UMA | 0   |

&lt;Core Design&gt;

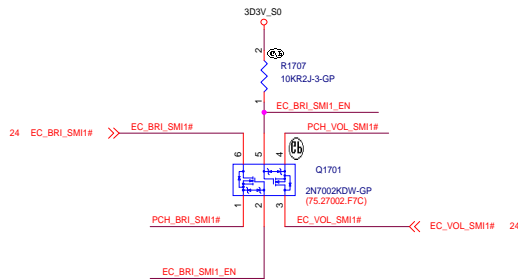
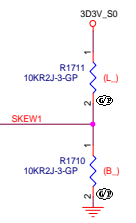
wistron  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsinchu, Taipei, Taiwan

Wistron Incorporated  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsinchu, Taipei, Taiwan

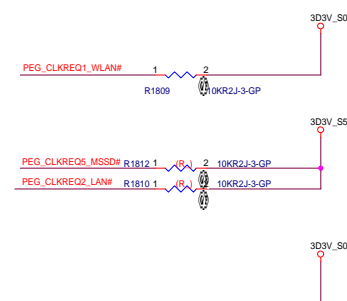
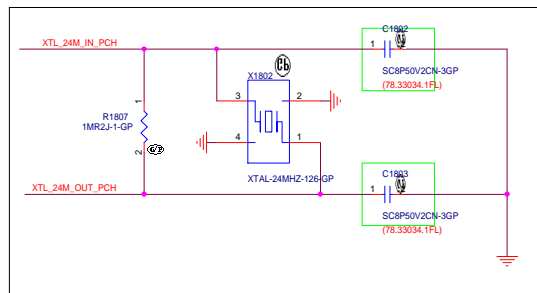
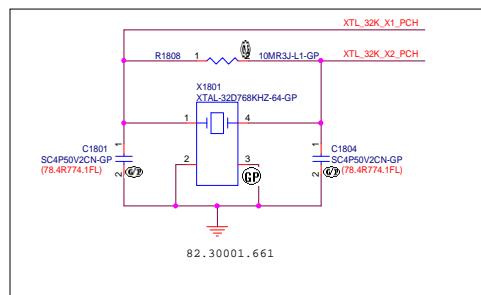
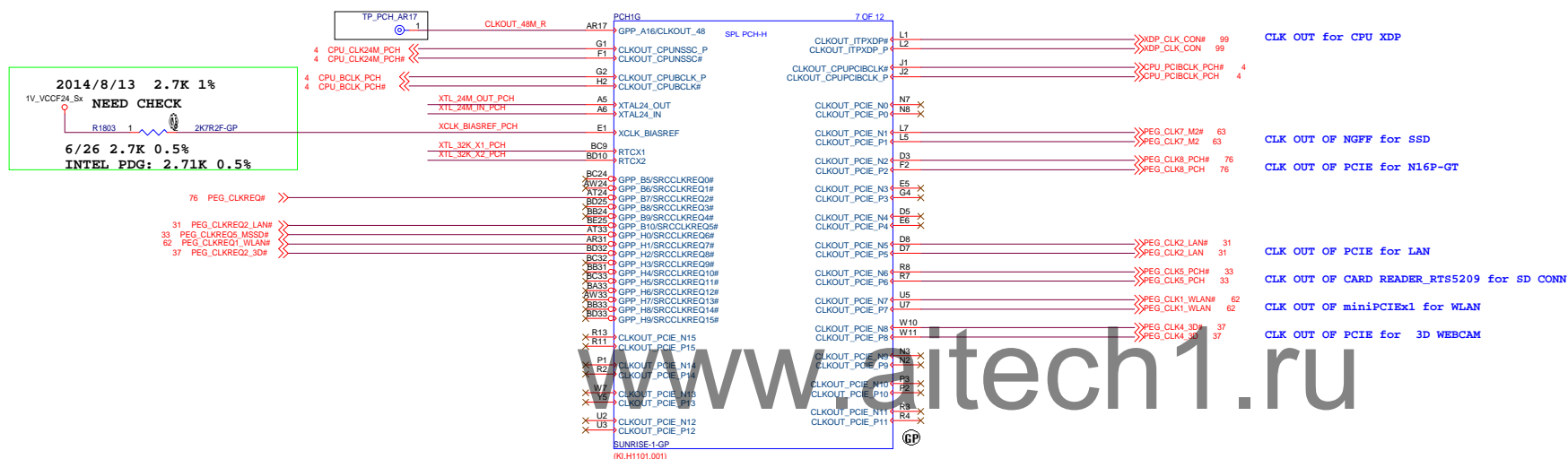
|       |                         |
|-------|-------------------------|
| Title | PCH (DMI/PCI-E/USB)     |
| Size  | Document Number         |
| C     | Consumer AIO Scotland   |
| Date  | Friday, August 21, 2015 |
| Sheet | 16 of 107               |



### SKEW ID



6/21 Delete  
CLKOUT\_48 is only supported and enabled on SKL-H Server



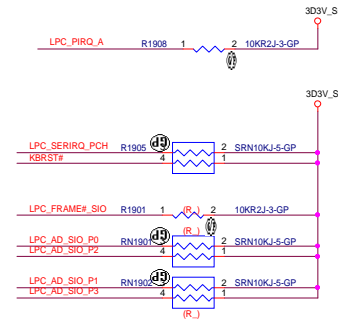
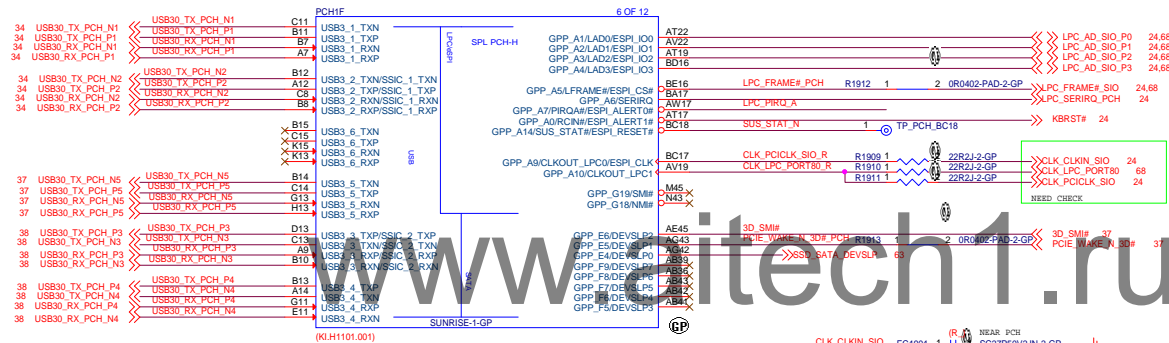
PORT1 USB30 SIDE PORT

PORT2 USB30 SIDE PORT

PORT5 USB30 3D WEBCAM

PORT3 USB30 REAR PORT

PORT4 USB30 REAR PORT



#### Integrated Pull-ups and Pull-downs

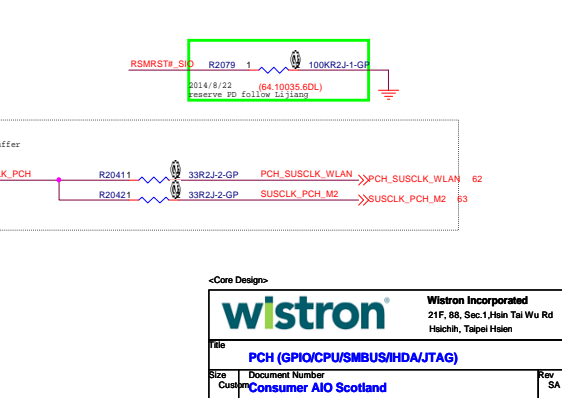
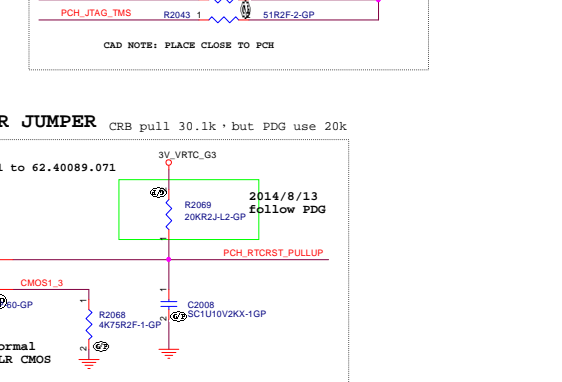
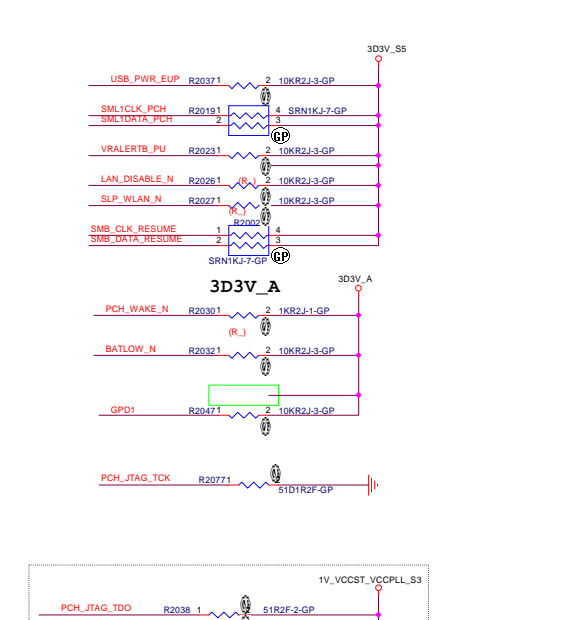
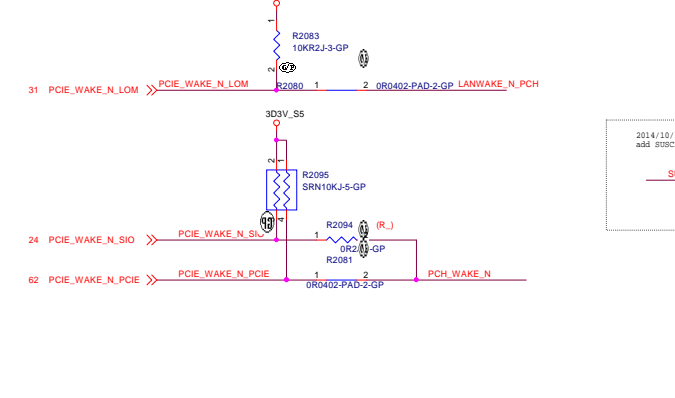
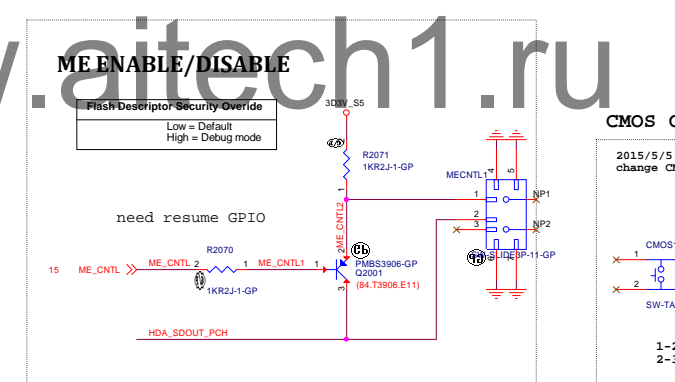
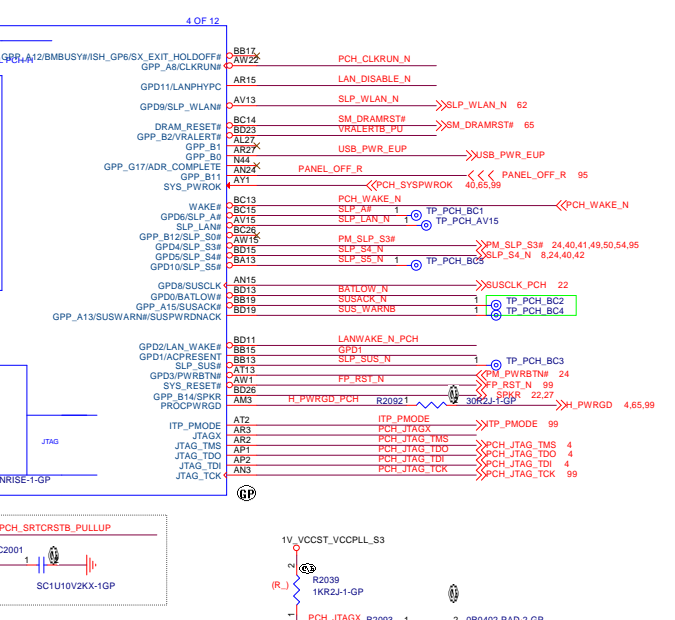
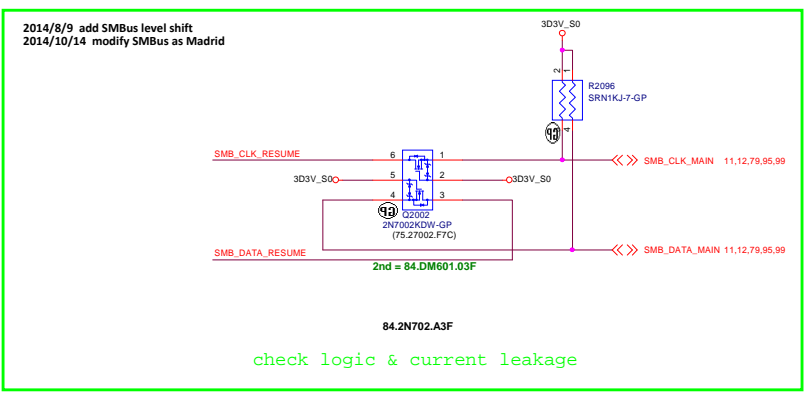
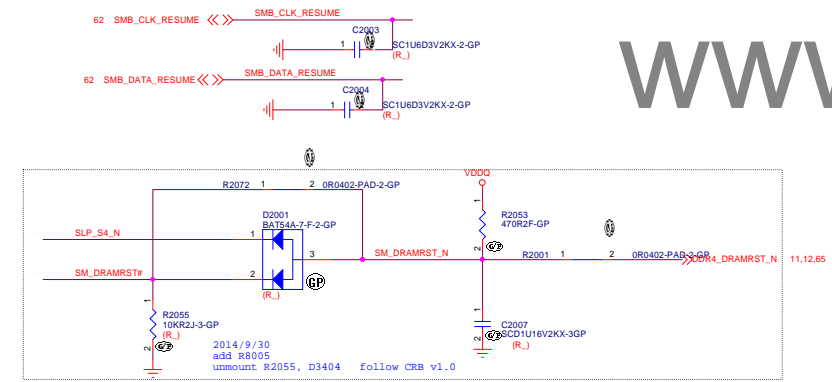
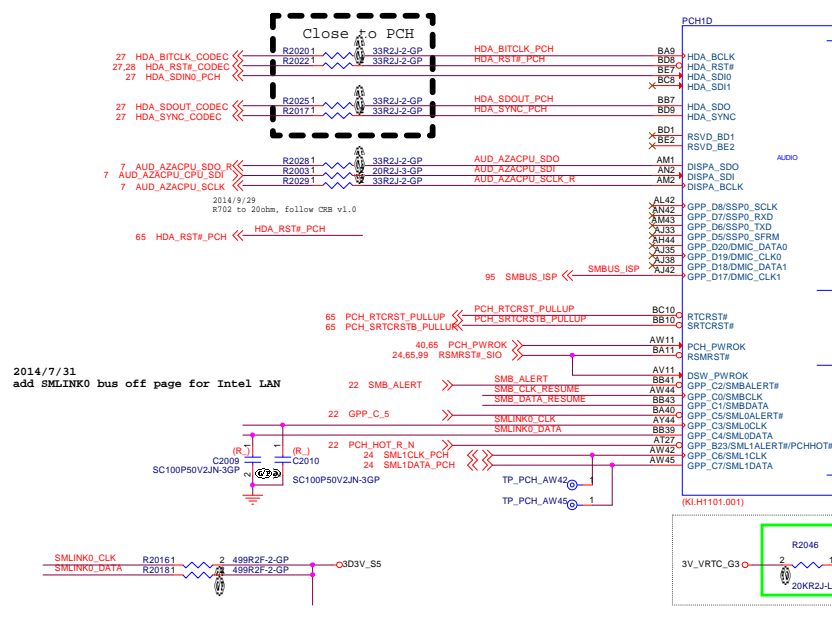
| Signal   | Resistor Type | Value      | Notes |
|----------|---------------|------------|-------|
| LAD[3:0] | Pull-up       | 15 ~ 40 KΩ |       |

<Core Design>

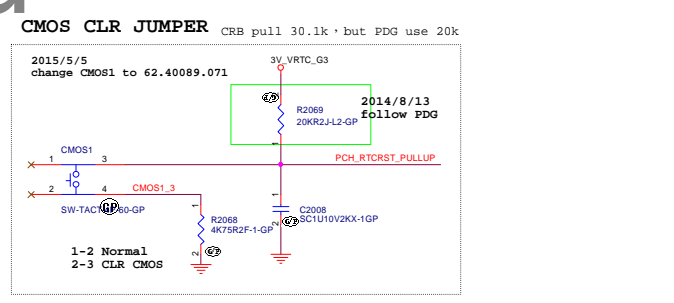
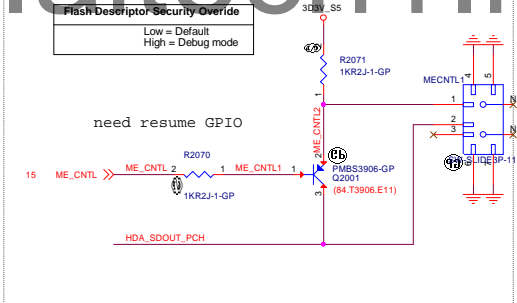
**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsinchu, Taipei Hsinchu

|                                  |   |           |           |
|----------------------------------|---|-----------|-----------|
| Title<br><b>PCH (USB/ESPI)</b>   |   |           | Rev<br>SA |
| Size<br>C                        | Document Number<br><b>Consumer AIO Scotland</b> |           |           |
| Date:<br>Friday, August 21, 2015 | Sheet<br>19                                     | of<br>107 |           |

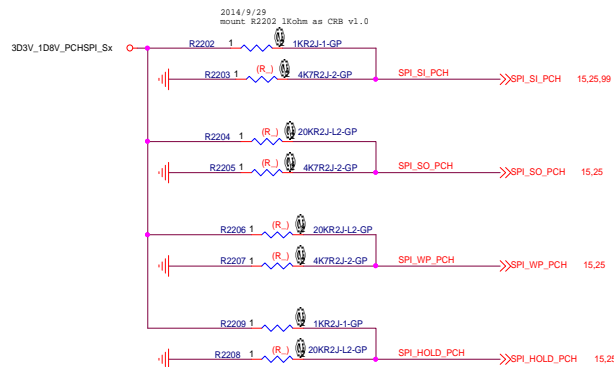


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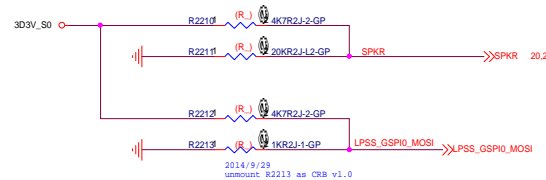




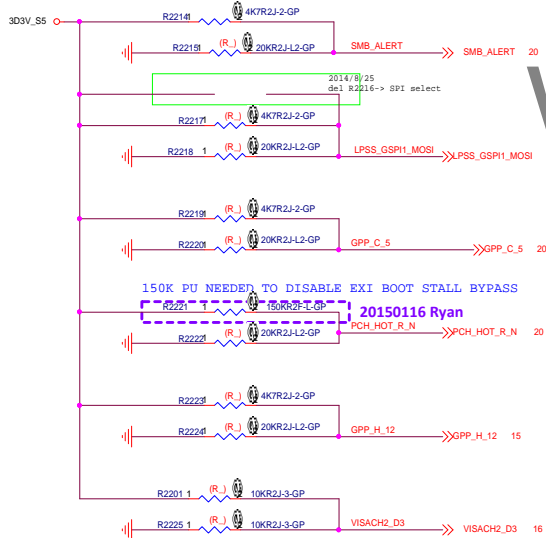
## PCH STRAP FUNCTIONS



|                            |   |
|----------------------------|---|
| SPI_SI_PCH<br>(SPI0_MOSI)  | 0: Enable boot halt<br>1: Disable boot halt<br>The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted. |
| SPI_SO_PCH<br>(SPI0_MISO)  | 0: Disable JTAG ODT<br>1: Enable JTAG ODT<br>The internal PU resistor is enabled when RSMRST# is asserted   |
| SPI_WP_PCH<br>(SPI0_IO2)   | 0: Enable consent strap<br>1: Disable consent strap<br>PCH has internal weak PU   |
| SPI_HOLD_PCH<br>(SPI0_IO3) | 0: Enable personality strap<br>1: Disable personality strap<br>PCH has internal weak PU   |



|   |   |
|---|---|
| SPKR<br>(SPKR / GPP_B14)                | 0: Disable Top Swap mode. (Default)<br>1: Enable Top Swap mode.<br>PCH internal pull-down is disabled after PLTRST# deasserts.                                      |
| LPSS_GSPI0_MOSI<br>(GPP_B18/GSPI0_MOSI) | 0: Disable No Reboot mode.<br>1: Enable No Reboot mode This function is useful when running ITP/XDP.<br>The internal pull-down is disabled after PLTRST# deasserts. |



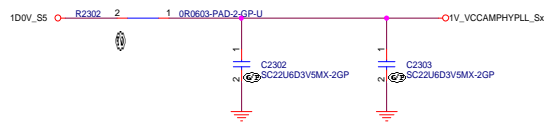
|   |   |
|---|---|
| PCH_PORT80_LED<br>(GPP_C2/SMBALERT#)        | 0: Disable TSL confidentiality<br>1: Enable TSL confidentiality (default)<br>The internal pull-down is disabled after RSMRST# deasserts.  |
| LPSS_GSPI1_MOSI<br>(GPP_B22/GSPI1_MOSI)     | BOOT SELECT STRAP<br>0: SPI select<br>1: LPC select<br>The internal pull-down is disabled after PLTRST# deasserts.  |
| GPP_C_5<br>(GPP_C5/SML0ALERT#)              | ESPI/LPC SELECT STRAP<br>0: LPC is selected for EC.<br>1: eSPI is selected for EC.<br>The internal pull-down is disabled after RSMRST# deasserts.                               |
| PCH_HOT_R_N<br>(GPP_B23/SML1ALERT#/PCHHOT#) | 0: Disable Exi boot stall bypass<br>1: Enable Exi boot stall bypass<br>The internal PD resistor is disable after RSMRST# de-asserted.   |
| GPP_H_12<br>(GPP_H12/SML2ALERT#)            | ESPI flash sharing mode<br>0: Master attached flash sharing<br>1: Slave attached flash sharing<br>PCH has internal weak PD.   |
| VISACH2_D3<br>(GPP_E12)                     | DFX test mode<br>0: XTAL input is single ended.<br>1: XTAL input is differential.<br>The internal PD resistoris disabled after RSMRST# de-asserts                               |
| HDA_SDOUT_PCH<br>(HDA_SDO)                  | 0: Enable security measures defined in the Flash Descriptor.<br>1: Disable Flash Descriptor Security (override).<br>The internal pull-down is disabled after PLTRST# deasserts. |
| SUSCLK_PCH<br>(GPD8/SUSCLK)                 | 0: Disable OD PLL VR<br>1: Enable OD PLL VR   |

Need check  
Though CRB use LPC to connect EC.  
This pin doesn't pull down

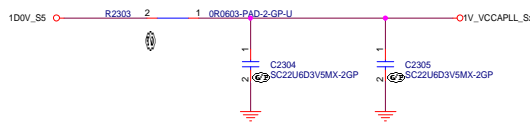
Follow ROSA / D7 triggerfish & Lily / M800 skylake project.



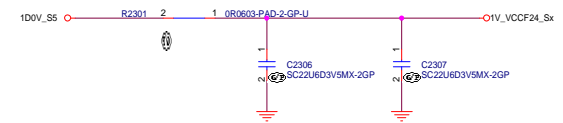
<Core Design>



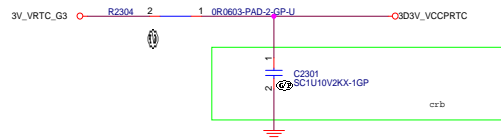
DESIGN NOTE:  
PLACE HOLDER FOR VCCMPHYPLL\_1P0 FILTER  
CAD NOTE:  
PLACE CLOSE TO PCH PIN  
PIN A42,A43, AND B43



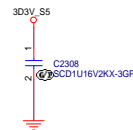
DESIGN NOTE:  
PLACE HOLDER FOR VCCAUSB\_1P0 AND VCCAAZPLL\_1P0 FILTER  
CAD NOTE:  
PLACE CLOSE TO PCH PIN  
PIN AJ5,AL5, AND AN19



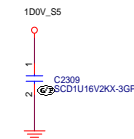
DESIGN NOTE:  
PLACE HOLDER FOR VCCF24\_1P0 FILTER  
CAD NOTE:  
PLACE CLOSE TO PCH PIN  
PIN K2 AND K3



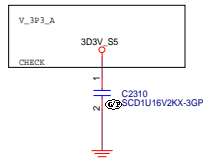
DESIGN NOTE:  
BOARD CAP FOR VCCPRTC\_3P3  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN BA22



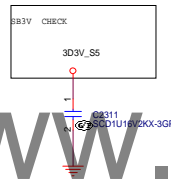
DESIGN NOTE:  
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN AJ41 AND AL41



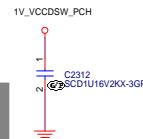
DESIGN NOTE:  
BOARD CAP FOR VCCMPHY\_1P0  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN U21,U23,U25,U26,V26



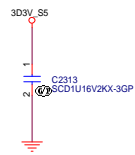
DESIGN NOTE:  
EDGE CAP FOR VCCPUSBD SW\_3P3  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN W15



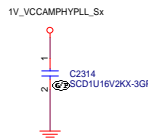
DESIGN NOTE:  
BOARD CAP FOR VCCPRTC PRIM\_3P3  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN BA20



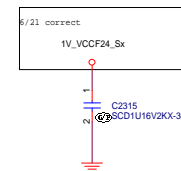
DESIGN NOTE:  
BOARD CAP FOR VCCDSW\_1P0  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN BA29



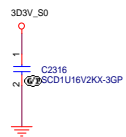
DESIGN NOTE:  
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN AD41



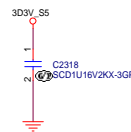
DESIGN NOTE:  
BOARD CAP FOR VCCMPHYPLL\_1P0(PLACE HOLDER)  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN A42,A43 AND B43



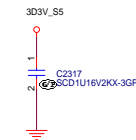
DESIGN NOTE:  
BOARD CAP FOR VCCF24\_1P0(PLACE HOLDER)  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN K2,K3



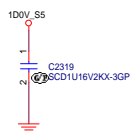
DESIGN NOTE:  
BOARD CAP FOR VCCATS  
CAD NOTE:  
PLACE 3~5MM FROM PACKAGE EDGE  
PIN AD13



DESIGN NOTE:  
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN BC42 AND BD40



DESIGN NOTE:  
BOARD CAP FOR VCCPHVC\_3P3(PLACE HOLDER)  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN AN15



DESIGN NOTE:  
EDGE CAP FOR VCCMPHY\_1P0 AND VCCDUSB\_1P0  
CAD NOTE:  
PLACE 1~3MM FROM PACKAGE EDGE  
PIN U21,U23,U25,U26,V26, AND AC17

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[illegible]

```
2014/8/6
add SPI1 62.10076.011
```

Single Flash Device: 15ohm  
Dual Flash Device: 33ohm

## SKL Platforms – SPI0\_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

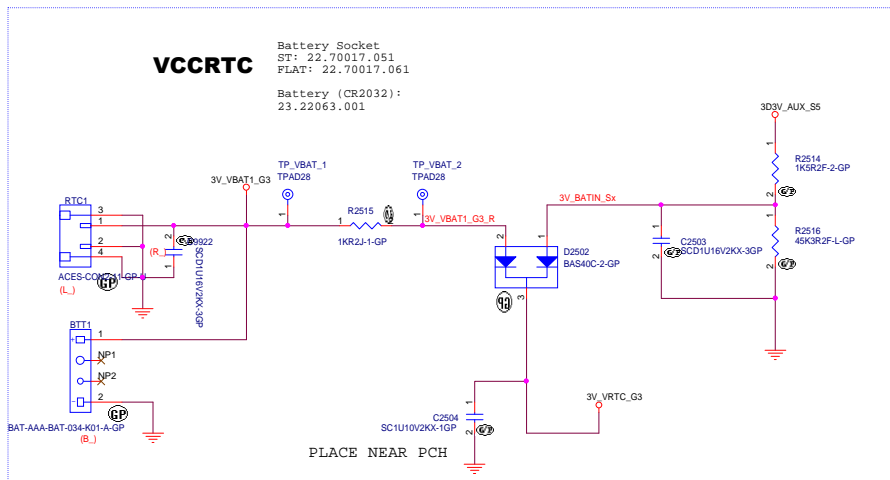
An Intel internal debug strap is implemented on the SPI0\_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

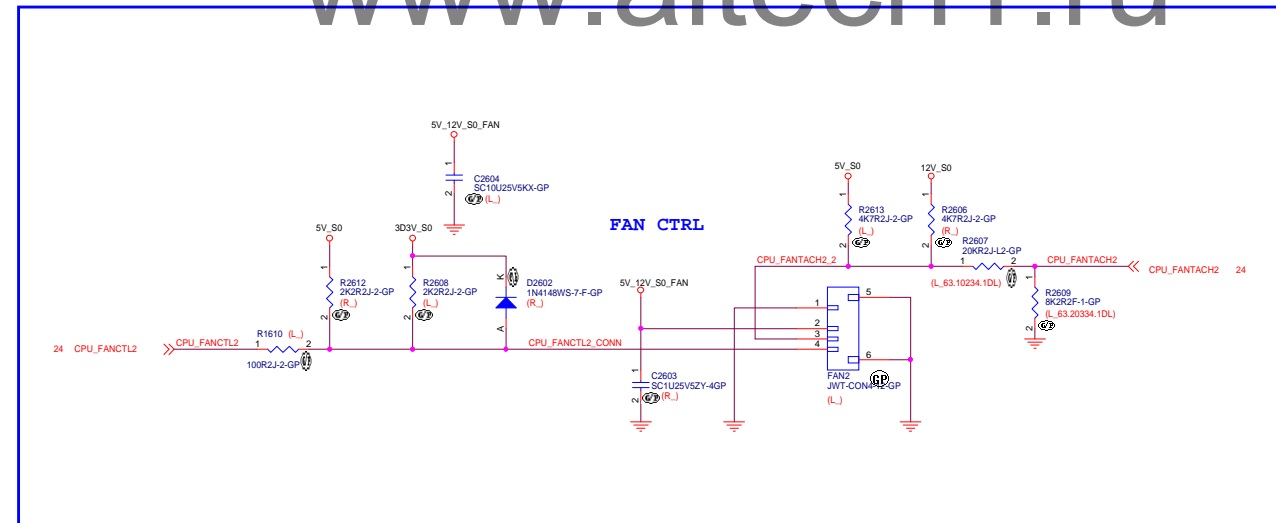
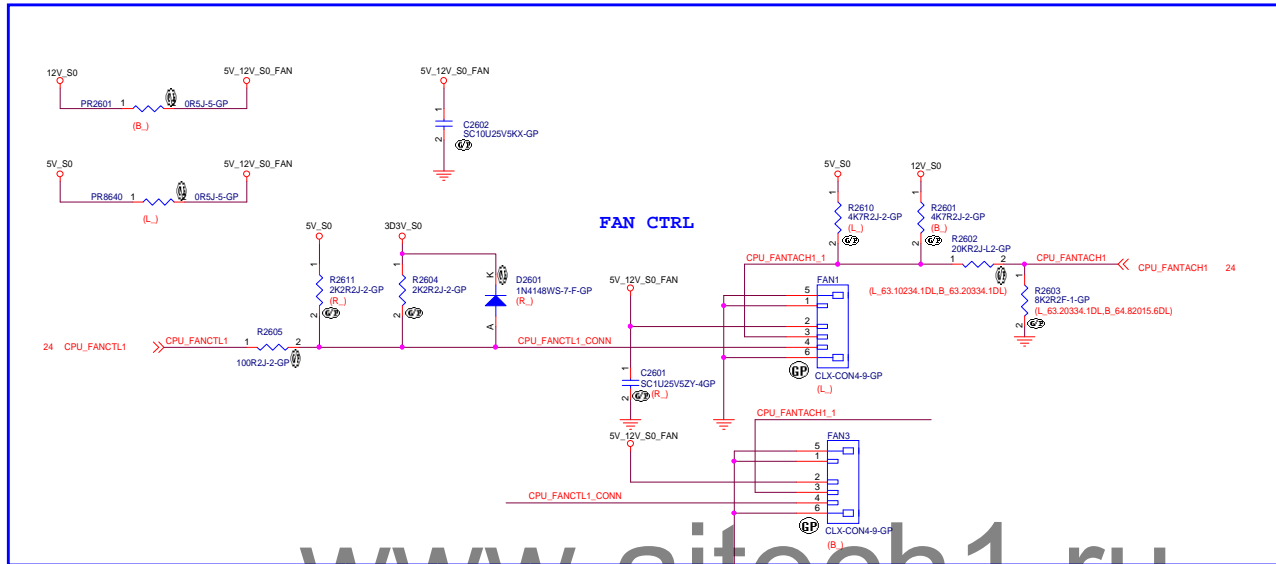
To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0\_TO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

**Option 1:** Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0\_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.





```

20  HDA_BITCLK_CODEC <==
20,28 HDA_RST#_CODEC <==
20  HDA_SDIN0_PCH <==

20  HDA_SDOUT_CODEC <==
20  HDA_SYNC_CODEC <==

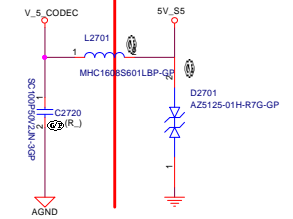
```

20,22 SPKR >>————

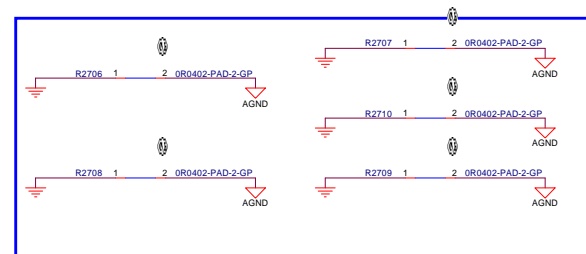
28 AMP\_CODEC\_PD &lt;&lt;-----

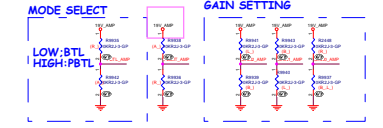
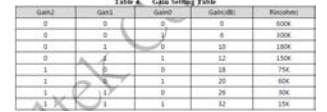
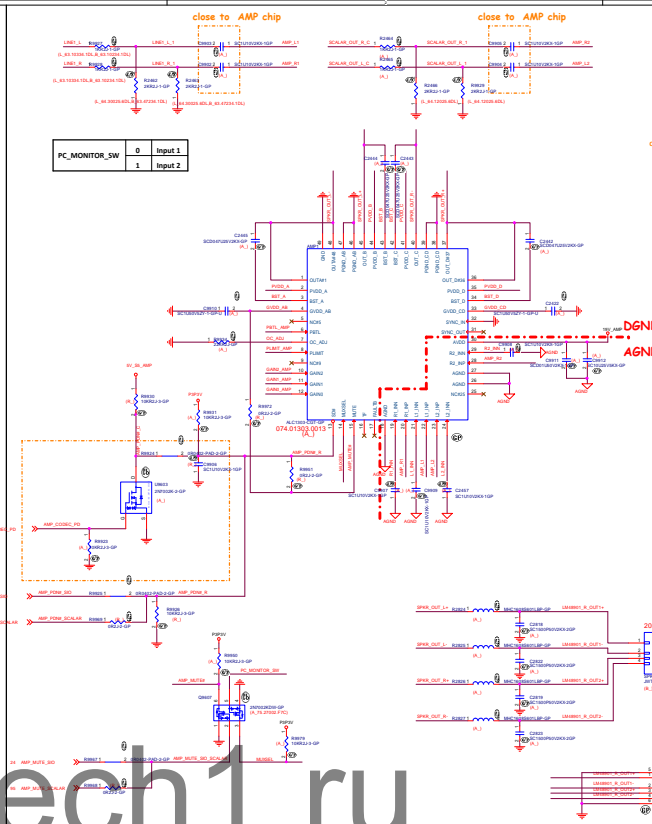
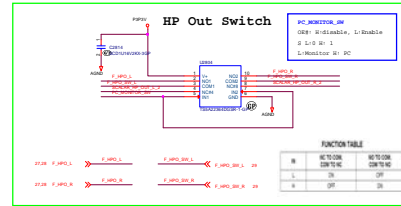
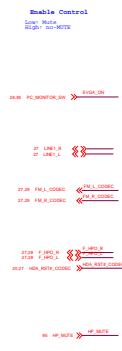
29 FM\_L\_CODEC << FM\_L\_CODEC

28 JD\_HP\_R &gt;&gt;————

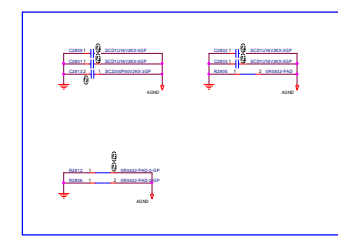
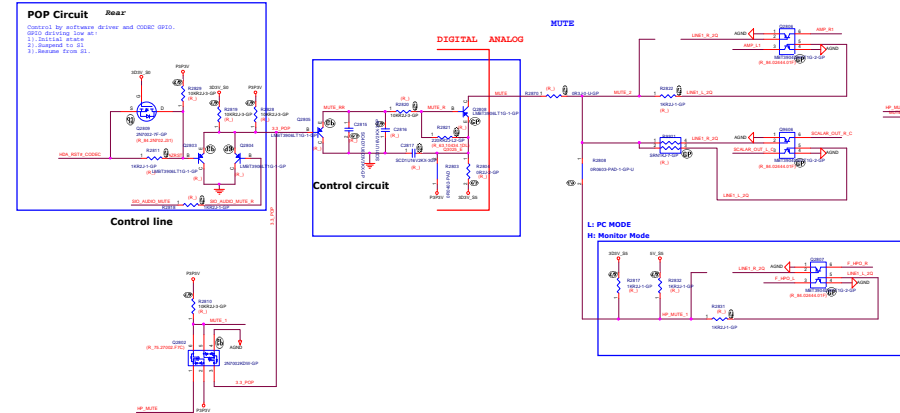


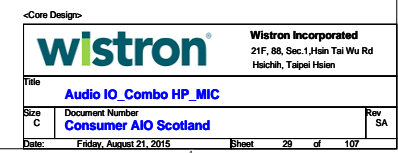
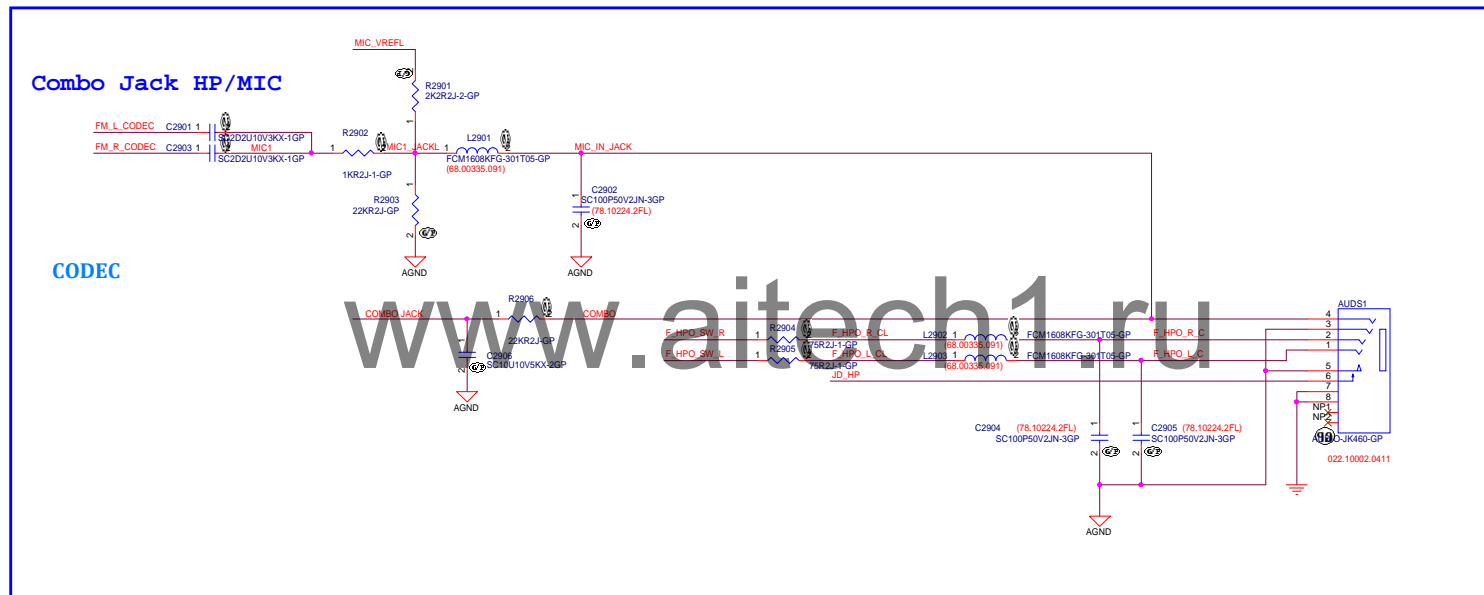
## Digital Moat

[illegible]



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|   |                         |
|---|-------------------------|
| <Core Design>   |                         |
|  <b>Wistron Incorporated</b><br>21F, 88, Sec.1,Hsin Tai Wu Rd<br>Hsichih, Taipei Hsien |                         |
| Title   |                         |
| RJ45&Transformer  |                         |
| Size  | Document Number         |
| C   | Consumer AIO Scotland   |
| Date:   | Friday, August 21, 2015 |
| Sheet   | 32 of 107               |
| Rev   | SA                      |



# USB3.0 SIDE Port: Co-lay USB 3.0 Type A (USBS1) & USBS3.0 Type C (USBS3) Channel Configuration

## USB3.0 SIDE CONNECTOR

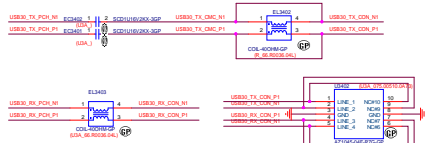


## Charger Function U1SB3.0 Type C

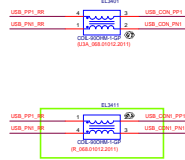


## Non Charger

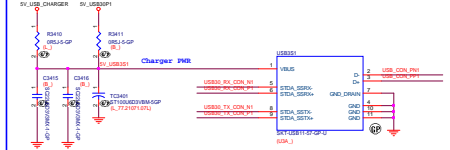
## USB3.0 EMI



## USB2.0 EMI

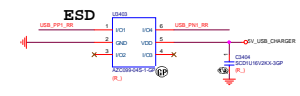


## USB3.0 Type A connector

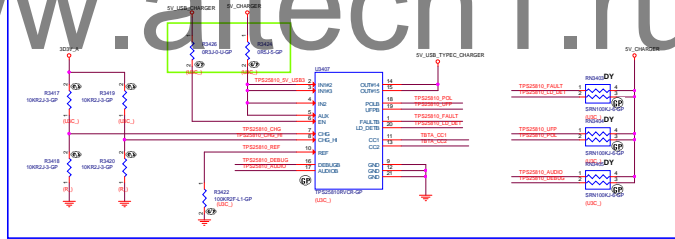
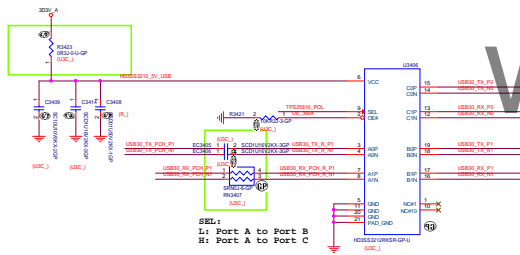


| Pin | Definition |
|-----|------------|
| 1   | POWER      |
| 2   | USB 3.0 D- |
| 3   | USB 3.0 D+ |
| 4   | NC         |
| 5   | NC         |
| 6   | NC         |
| 7   | NC         |
| 8   | NC         |
| 9   | NC         |

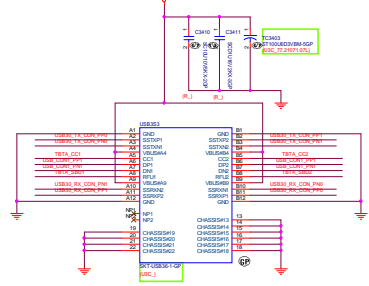
## USB3.0's USB2 pair from PCH



## USB3.0 SIDE Type C Channel Configuration

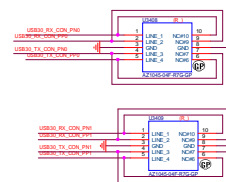
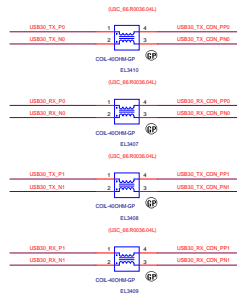
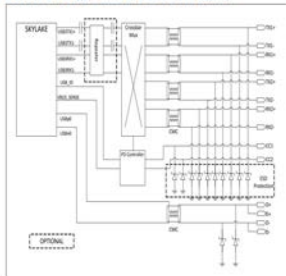


## USB3.0 Type C connector



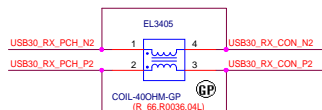
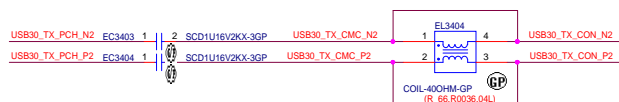
| CC1  | CC2  | PO4b    | Status        | TypeC USB 3.0 connection | MD365212    |
|------|------|---------|---------------|--------------------------|-------------|
| Open | Open | HL-s(H) | UFP connected | Root to SPTX1            | Port A to C |
| Open | Open | HL-s(H) | UFP connected | Root to SPTX2            | Port A to B |

Figure 1-9. USB 3.0 Only USB Type-C Connector (with Dual Role Support)



## USB3.0 SIDE PORT2

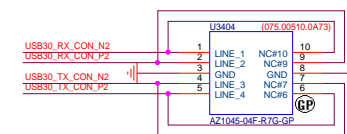
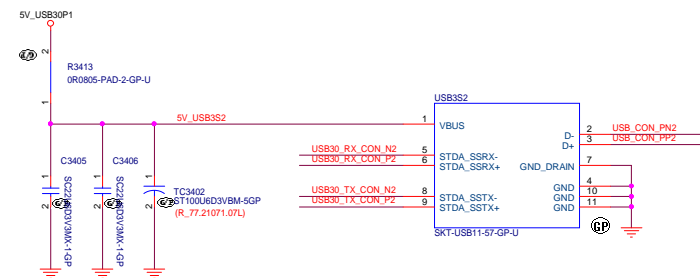
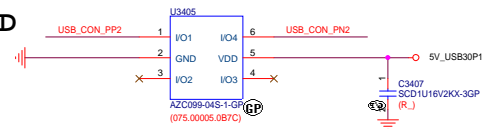
### USB3.0 EMI



### USB2.0 EMI



### ESD



19 USB30\_RX\_PCH\_N2  
19 USB30\_RX\_PCH\_P2  
19 USB30\_TX\_PCH\_N2  
19 USB30\_TX\_PCH\_P2

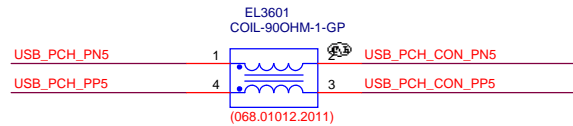
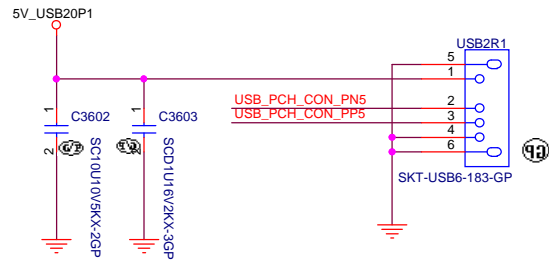
16 USB\_PCH\_PP2  
16 USB\_PCH\_PN2

Reserved

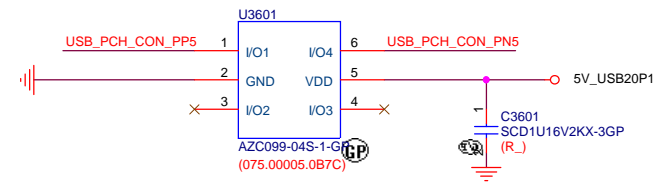
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## USB Port5

16 USB\_PCH\_PP5  
16 USB\_PCH\_PN5



### ESD



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<Core Design>

**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title  
**USB 20\_REAR PORT**

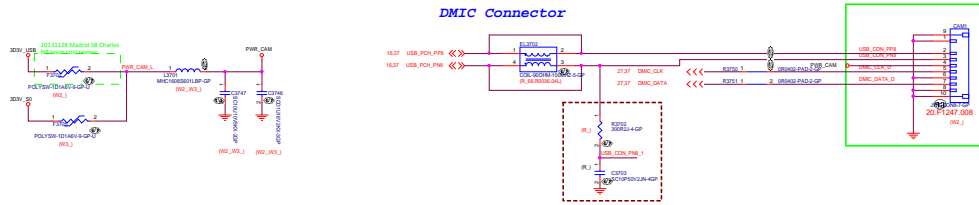
Size Document Number  
Customer **Consumer AIO Scotland**

Date: Friday, August 21, 2015

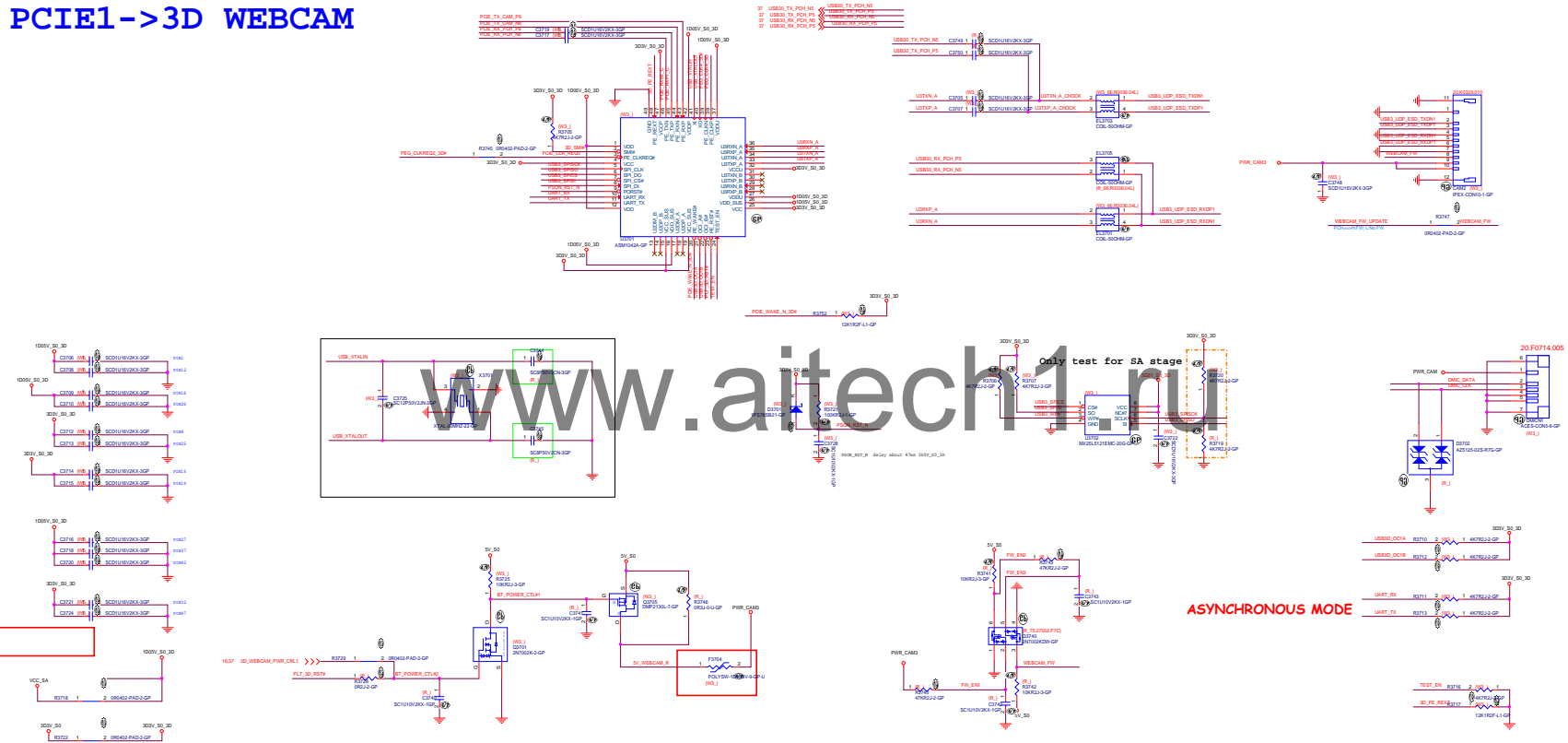
Sheet 36 of 107

Rev  
SA

## USB Port8 -> WEBCAM



## PCIE1->3D WEBCAM

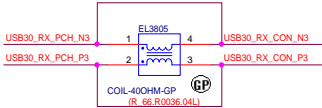
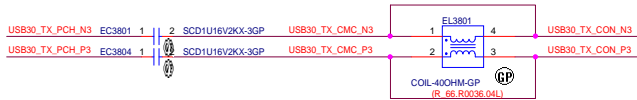


## USB Port7 -> Touch

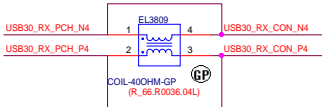
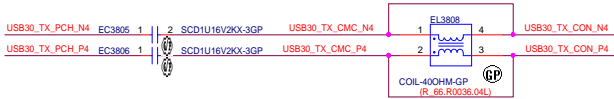


USB3.0 REAR CONNECTOR

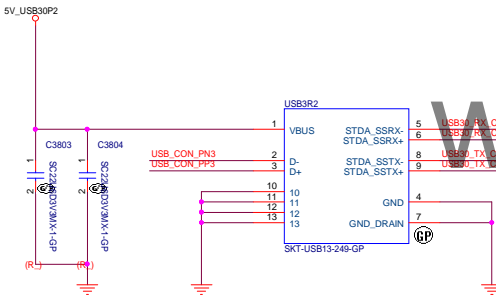
USB3.0 EMI



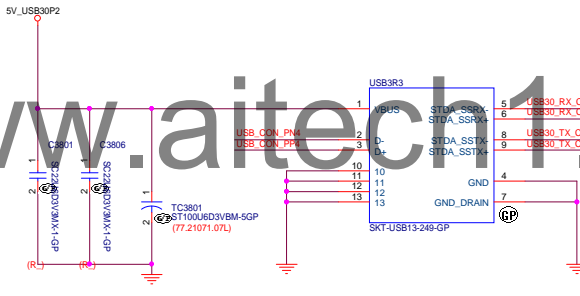
USB3.0 EMI



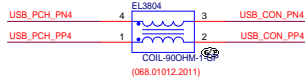
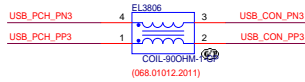
USB3.0 REAR PORT3



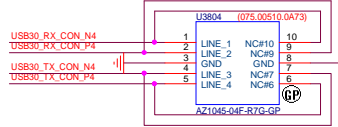
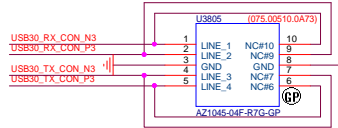
USB3.0 REAR PORT4



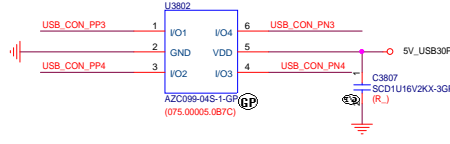
USB2.0 EMI



ESD

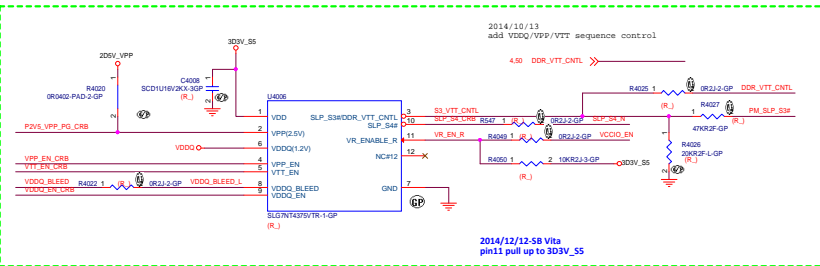


ESD

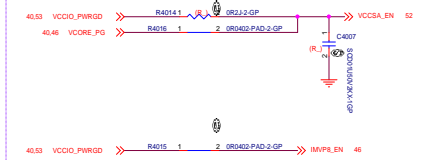
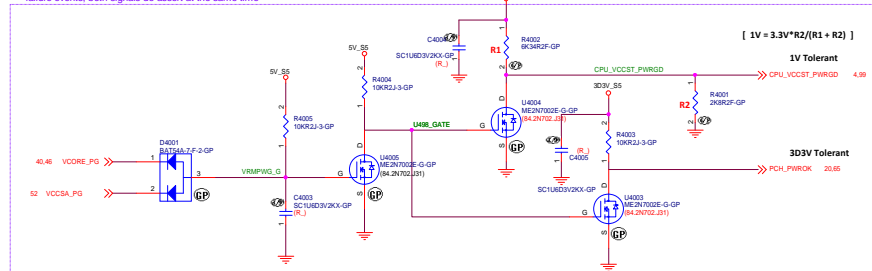


| USB 3.0 Connector<br>Pin definition |                          |
|-------------------------------------|--------------------------|
| 1                                   | POWER                    |
| 2                                   | USB 2.0 D-               |
| 3                                   | USB 2.0 D+               |
| 4                                   | GND                      |
| 5                                   | StdA_SSRX- SuperSpeed RX |
| 6                                   | StdA_SSRX+               |
| 7                                   | GND                      |
| 8                                   | StdA_SSTX- SuperSpeed TX |
| 9                                   | StdA_SSTX+               |

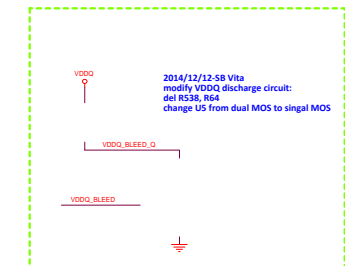
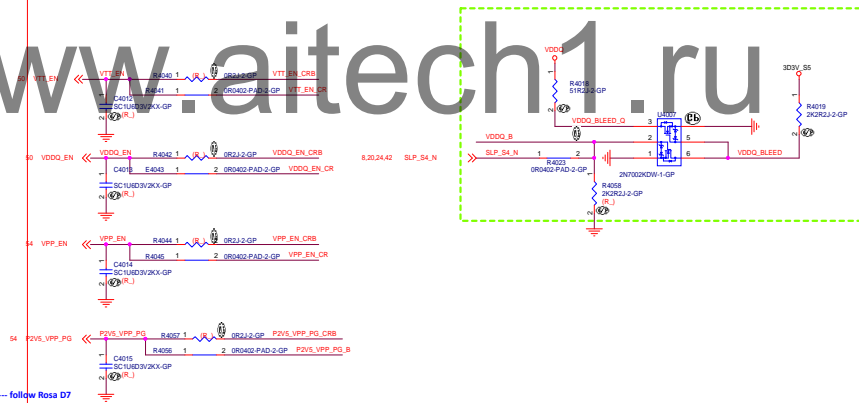
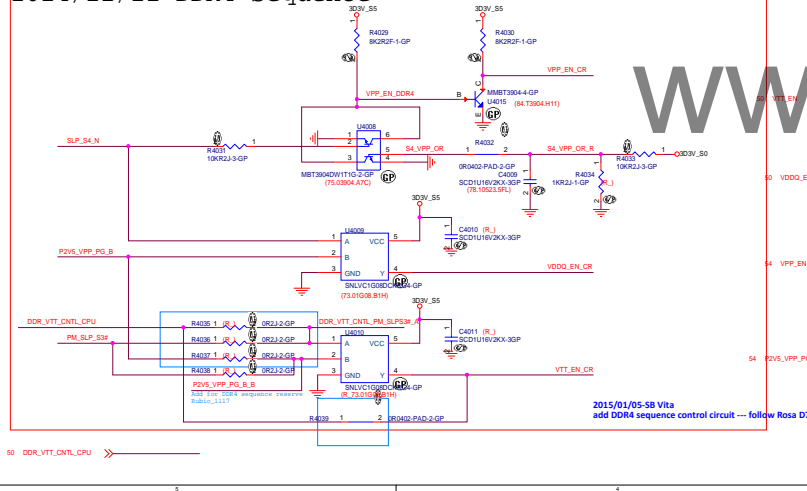
Reserved  
www.aitech1.ru



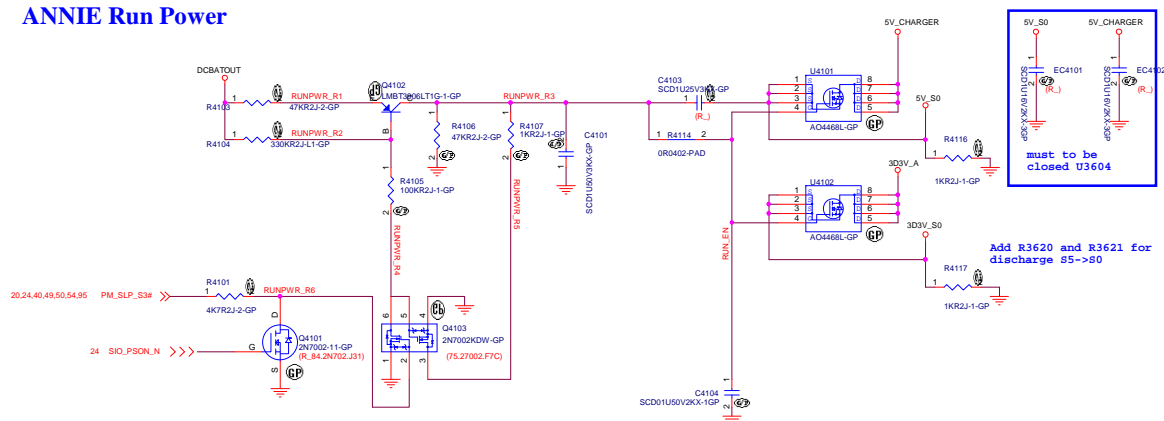
Note:  
VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it. It is recommended that both VCCST\_PWRGD and PCH\_PWROK include ALL\_SYS\_PWRGD and / or SLP\_S3# in their generation. This ensures during failure events, both signals de-assert at the same time



- 2014/11/11 DDR4 Sequence



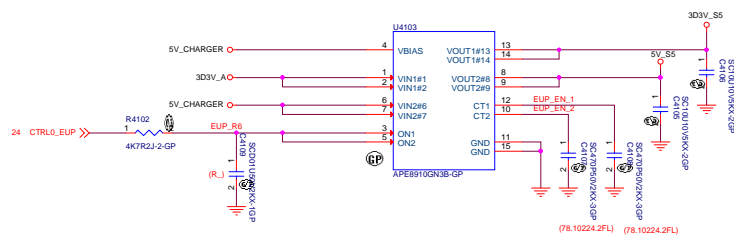
## ANNIE Run Power



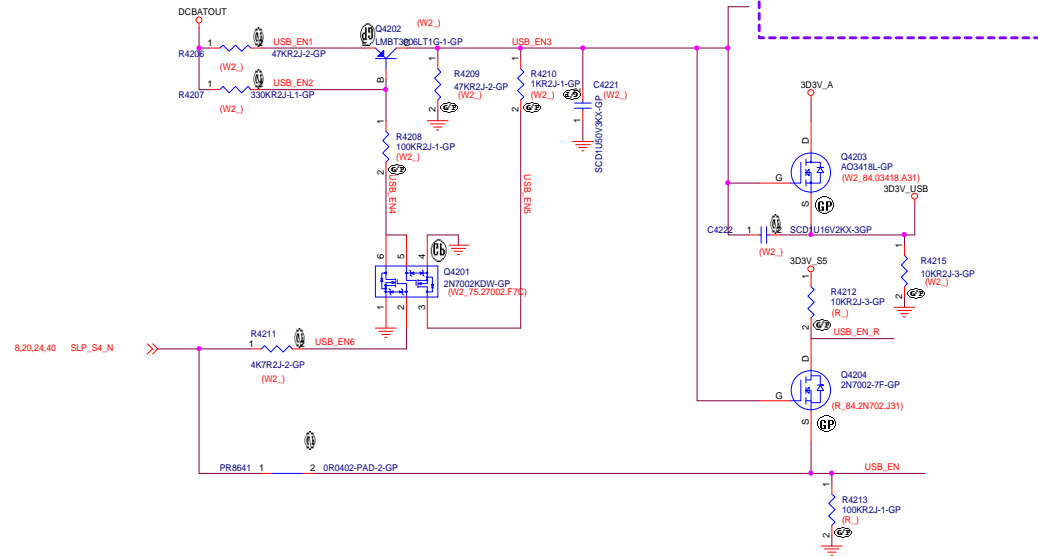
### EUP Power

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### Modify 3V/5V Logic Control as Load Switch

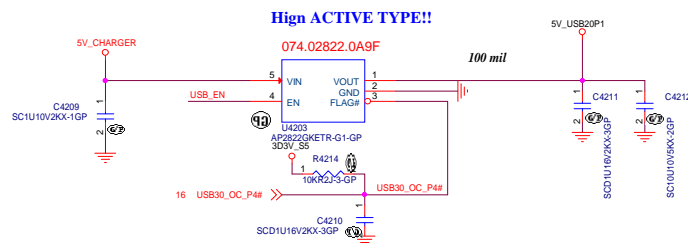
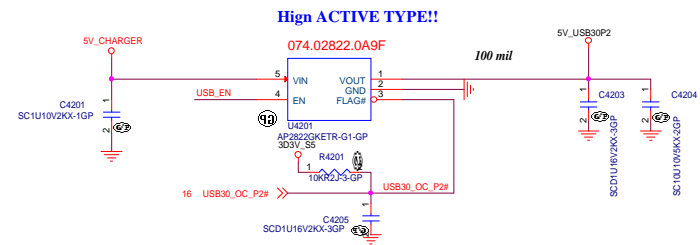
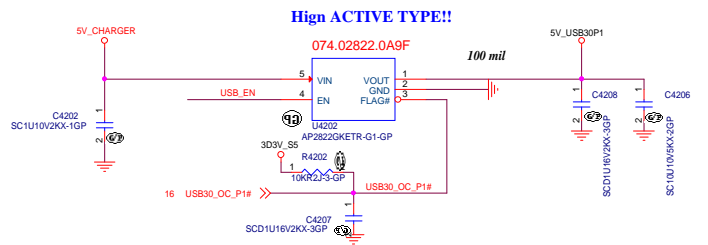


## VCC5\_USB

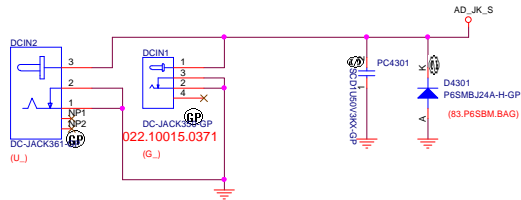


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### colay USB3S1 charger power

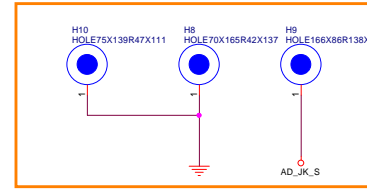


## ANNIE solution



20141216 DCIN1 PN Change to 022.10015.0371

20141216 Add H8-10 for DCIN1~2 match of power,ground pin



SIZE 2512  
0.010HM 2W

$$\text{GAIN1} = \text{VO} / (\text{V2} - \text{V1}) = \text{R2} / \text{R1}$$

$$\text{GAIN2} = 1 + \text{R2} / \text{R1}$$

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0P\_1071D.B0L  
Alt:

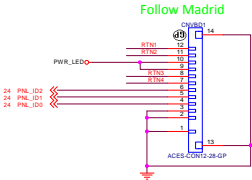
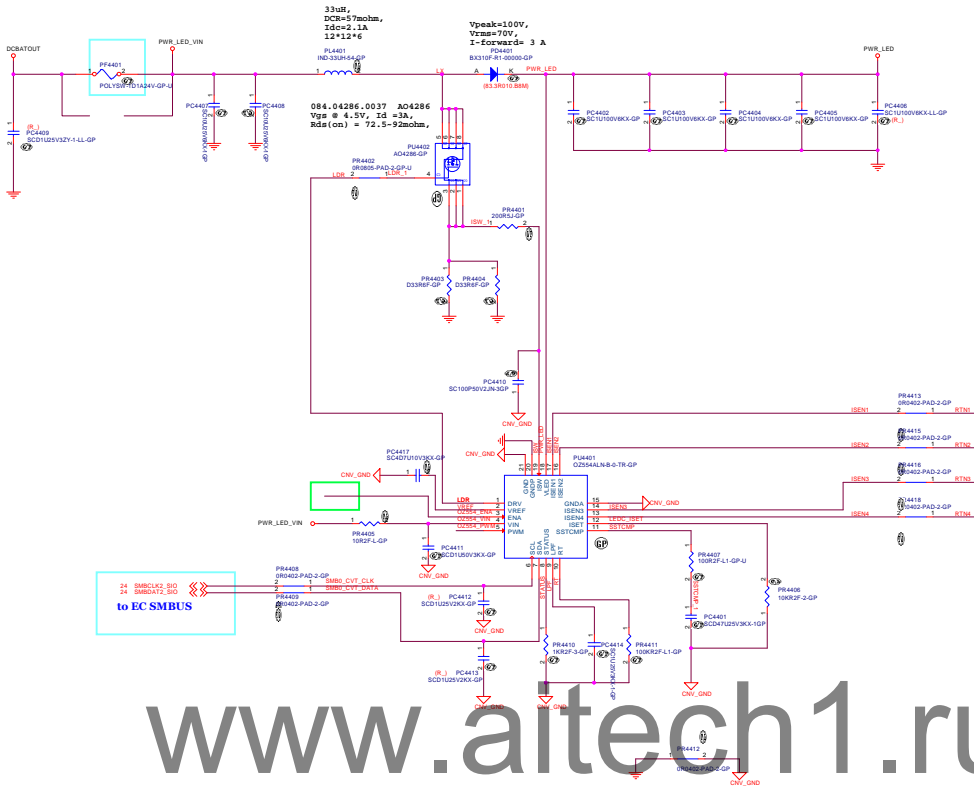
| RH          | Vc   | 10%   |
|-------------|------|-------|
| 135W: 6.04k | 5V   | ~121W |
| 90W: 6.04k  | 3.3V | ~81W  |
| 65W: 0      | 3.3V | ~60W  |

R4310 64.10025.6DL (for 135W)  
R4311 64.10025.6DL (for 90W)

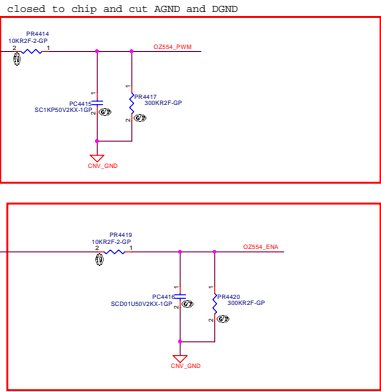
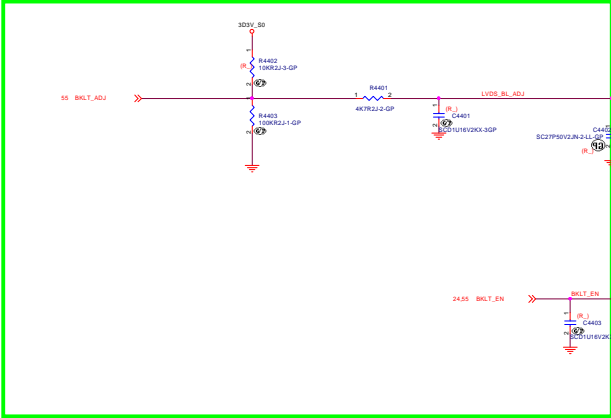
<Core Design>

Converter Board

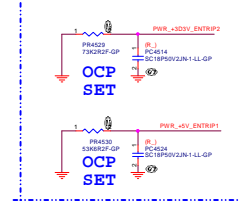
| Cable detection |            |            |              |
|-----------------|------------|------------|--------------|
| PANEL_SEL1      | PANEL_SEL2 | PANEL_SEL3 | Status       |
| 1               | 1          | 1          | Panel unplug |
| X               | X          | X          | Panel plug   |



Need EE to check

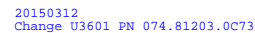


| Panel Model | Cable Spec |     |     |      |
|-------------|------------|-----|-----|------|
|             | ID0        | ID1 | ID2 | Vout |
|             | 0          | 0   | 0   |      |
|             | 0          | 0   | 1   |      |
|             | 0          | 1   | 0   |      |
|             | 1          | 0   | 0   |      |
|             | 1          | 1   | 0   |      |
|             | 1          | 1   | 1   |      |



| INLDO(V)        | SECFB           | ENTRIP1 | ENTRIP2 | LDOS(V) | LDQI(V) | SMP1 | SMP2 |
|-----------------|-----------------|---------|---------|---------|---------|------|------|
| >1.6V<br>=>High | LOW             | X       | X       | OEE     | OEE     | OEE  | OEE  |
| >1.6V<br>=>High | LOW             | X       | X       | On      | On      | OEE  | OEE  |
| >1.6V<br>=>High | OEE             | OEE     | OEE     | On      | On      | OEE  | OEE  |
| >1.6V<br>=>High | >2.3V<br>=>High | On      | On      | On      | On      | OEE  | On   |
| >1.6V<br>=>High | >2.3V<br>=>High | On      | On      | On      | On      | OEE  | On   |
| >1.6V<br>=>High | >2.3V<br>=>High | On=>PD  | On=>PD  | On      | On      | On   | On   |
| >1.6V<br>=>High | >2.3V<br>=>High | On      | OEE     | On      | On      | On   | On   |

## Intel SKYLAKE IMVP8 POWER 35W

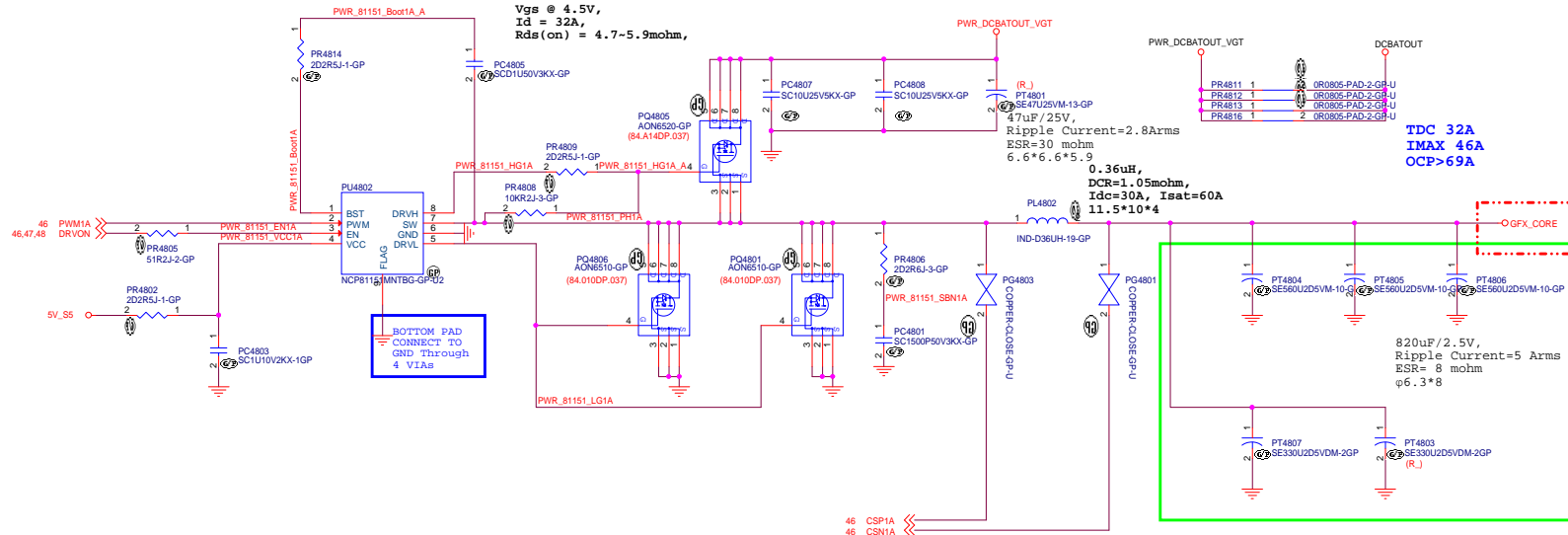




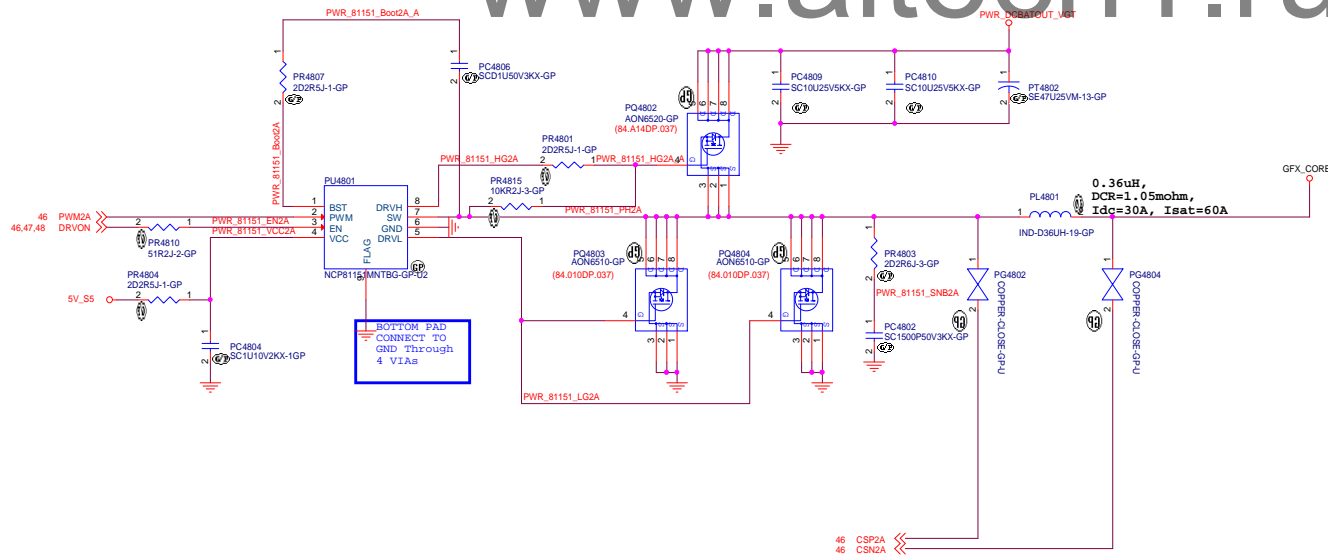
# PWR\_VCCGT

84.06520.037 AON6520  
Vgs @ 4.5V,  
Id = 29A,  
Rds(on) = 8.5-11mohm,

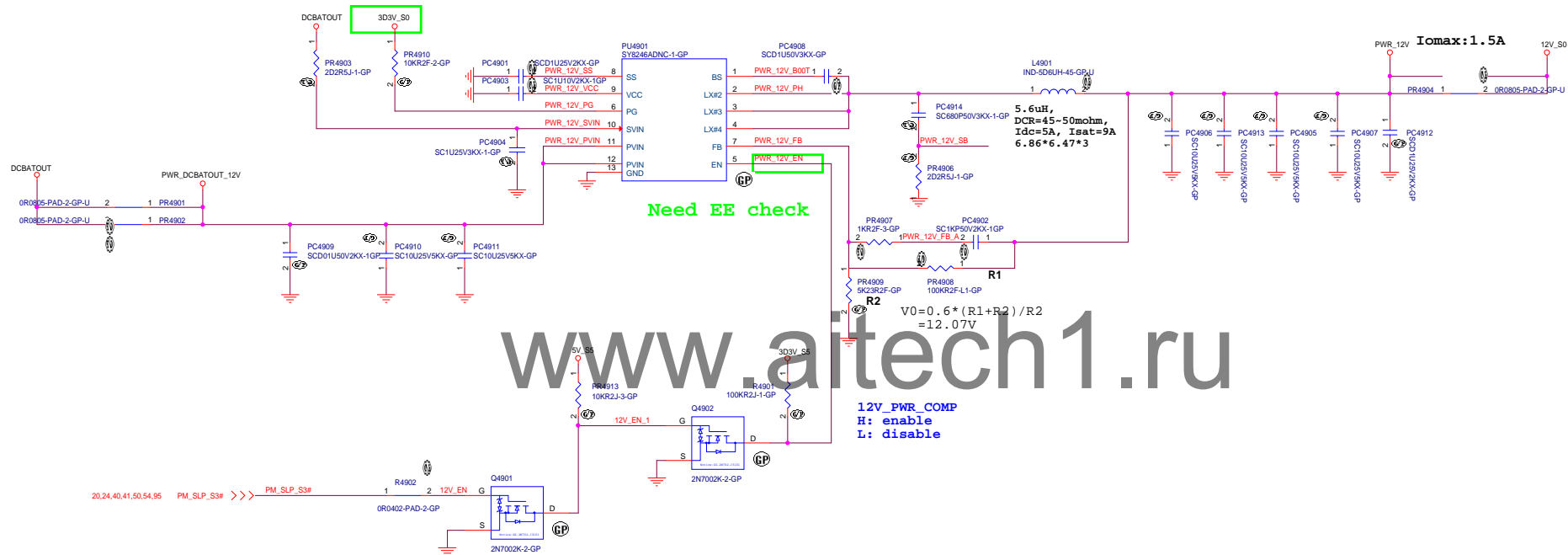
084.06510.0037 AON6510  
Vgs @ 4.5V,  
Id = 32A,  
Rds(on) = 4.7-5.9mohm,



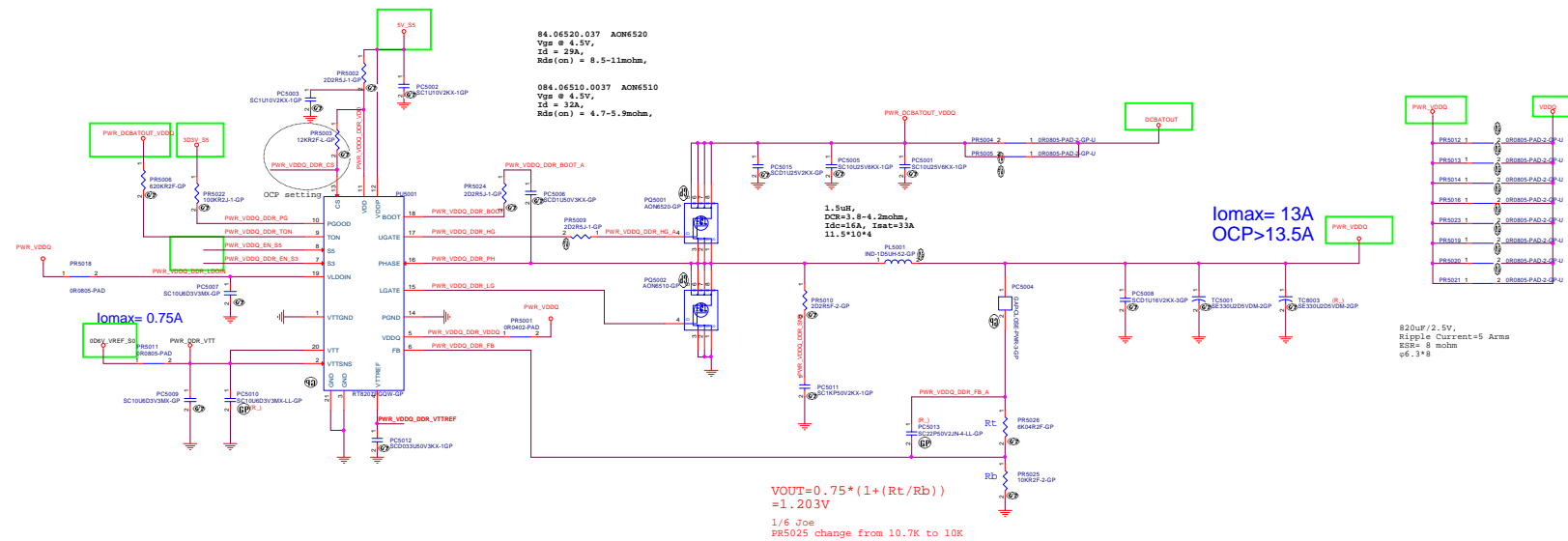
www.aitech1.ru



# PWR\_12V

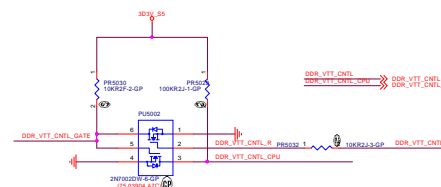
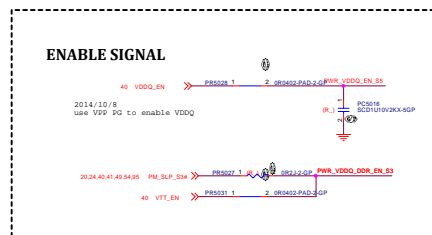


## PWR\_VDDQ



## ENABLE SIGNAL

[www.aitech1.ru](http://www.aitech1.ru)





# PWR\_VCCSA

Need EE to check

84.06520.037 AON6520  
Vgs @ 4.5V,  
Id = 29A,  
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510  
Vgs @ 4.5V,  
Id = 32A,  
Rds(on) = 4.7~5.9mohm,

FOR EMI

PWR\_DCBATOUT\_VCCSA  
PC5218  
SCD1U50V3KX-GP

PWR\_DCBATOUT\_VCCSA  
DCBATOUT  
PR5223 1  
PR5224 1  
OR0805-PAD-2-GP-U  
OR0805-PAD-2-GP-U

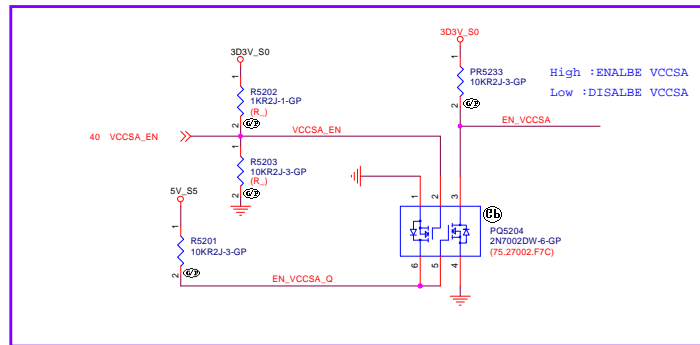
Iomax= 11.5A  
OCP>17.25A

0.82uH,  
DCR=6.7-8mohm,  
Idc=13A, Isat=24A  
6.86\*6.47\*3


470uF/2V,  
Ripple Current=3.5Arms  
ESR= 6 mohm  
7.3\*4.3\*1.9

$V_{OUT} = ((R1+R2)/R2)*0.704$   
 $= 0.704*(1+16.2/33)$   
 $= 1.05V$

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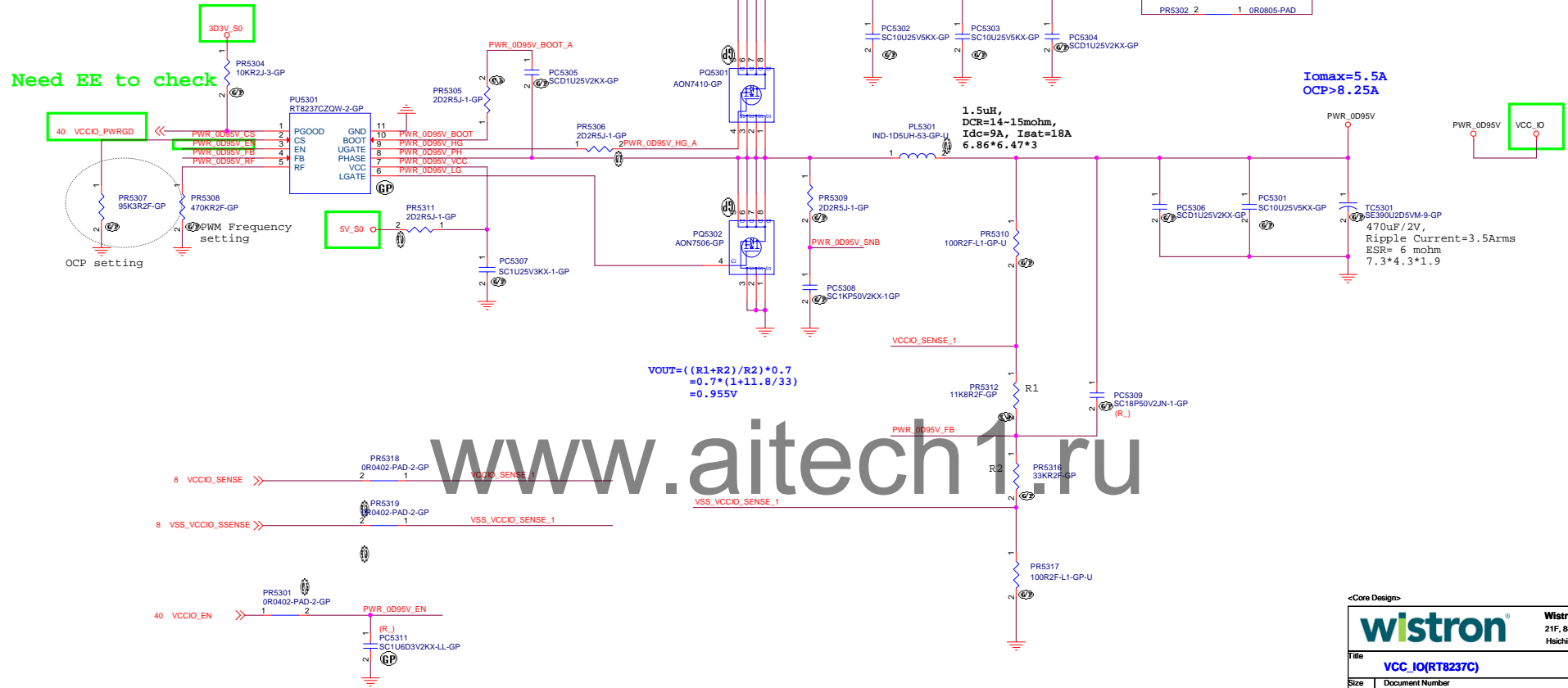
<Core Design>

|   |  |  |                 |
|---|--|--|-----------------|
|  |  | Wistron Incorporated<br>21F, 88, Sec.1 Hsin Tai Wu Rd<br>Hsichih, Taipei Hsien |                 |
| File<br>VCC_SA(RT8237C)   |  |  |                 |
| Size  | Document Number<br>Consumer AIO Scotland |  | Rev<br>SA       |
| Date  | Friday, August 21, 2015                  |  | Sheet 52 of 107 |

# PWR\_VCCIO

84.07410.A37 SIS412DN  
Vgs @ 4.5V,  
Id = 7A,  
Rds(on) = 24-29mohm,

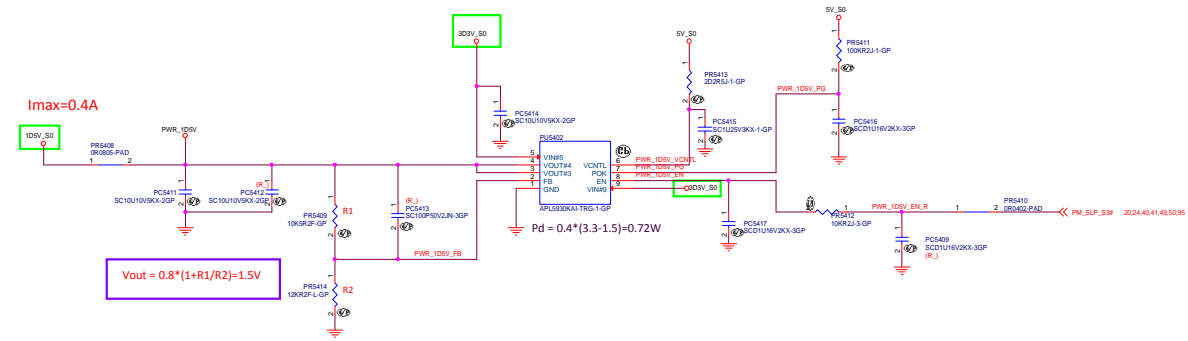
84.07506.037 AON7506  
Vgs @ 4.5V,  
Id = 10A,  
Rds(on) = 13-15.8mohm,



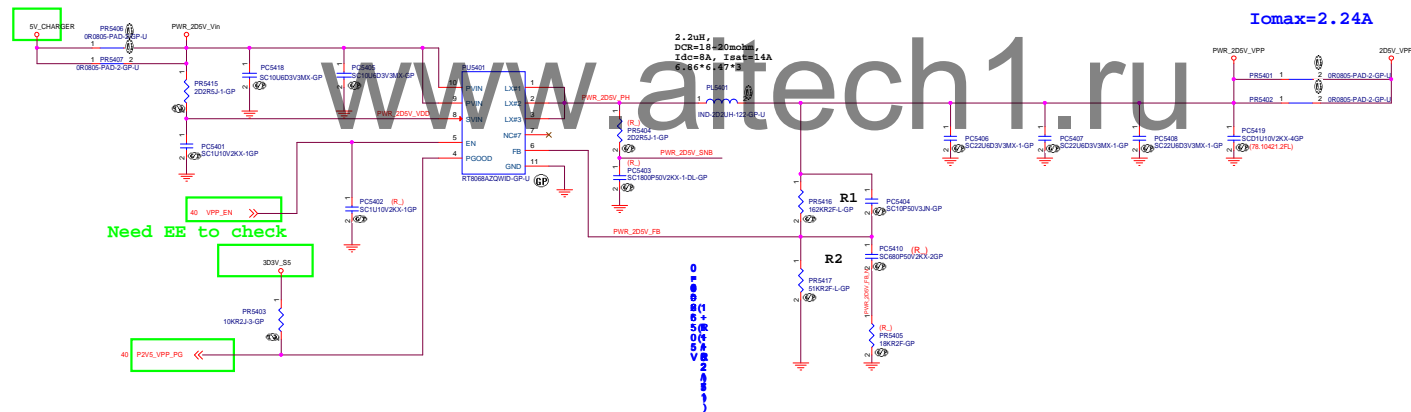
<Core Design>

|                        |                         |                                |           |
|------------------------|-------------------------|--------------------------------|-----------|
| <b>wistron</b>         |                         | <b>Wistron Incorporated</b>    |           |
|                        |                         | 21F, 88, Sec.1, Hsin Tai Wu Rd |           |
|                        |                         | Hsichih, Taipei Hsien          |           |
| Title                  |                         |                                |           |
| <b>VCC_IO(RT8237C)</b> |                         |                                |           |
| Size                   | Customer                | Document Number                | Rev       |
|                        |                         | <b>Consumer AIO Scotland</b>   | SA        |
| Date:                  | Friday, August 21, 2015 | Sheet                          | 53 of 107 |

## LDO: PWR\_1D5V



## PWR\_2D5V\_VPP



<Core Design>

|                                  |                         |                         |           |
|----------------------------------|-------------------------|-------------------------|-----------|
| wistron                          |                         | Wistron Incorporated    |           |
| 21F, 8B, Sec. 1, Hsin Tai Wu Rd. |                         | Hsinchu, Taipei, Taiwan |           |
| Rev                              | LDO_1P5V_1P8V_2P5V      | Rev                     | 5A        |
| Doc                              | Consumer AIO Scotland   | Rev                     | 5A        |
| Date                             | Friday, August 21, 2015 | Sheet                   | 54 of 107 |

```
SSID = VIDEO
```

## LVDS

|          |       |
|----------|-------|
| 95 TXD0- | TXD0- |
| 95 TXD0+ | TXD0+ |
| 95 TXD1- | TXD1- |
| 95 TXD1+ | TXD1+ |
| 95 TXD2- | TXD2- |
| 95 TXD2+ | TXD2+ |
| 95 TXD3- | TXD3- |
| 95 TXD3+ | TXD3+ |
|          |       |
| 95 TXE0- | TXE0- |
| 95 TXE0+ | TXE0+ |
| 95 TXE1- | TXE1- |
| 95 TXE1+ | TXE1+ |
| 95 TXE2- | TXE2- |
| 95 TXE2+ | TXE2+ |
| 95 TXE3- | TXE3- |
| 95 TXE3+ | TXE3+ |

```

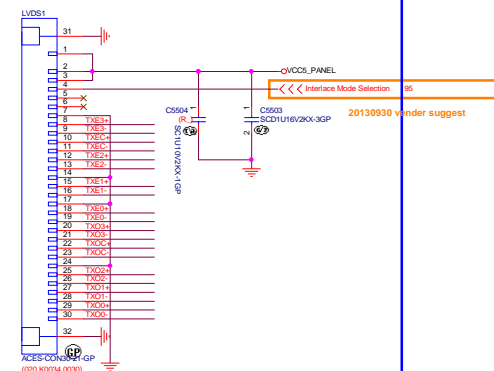
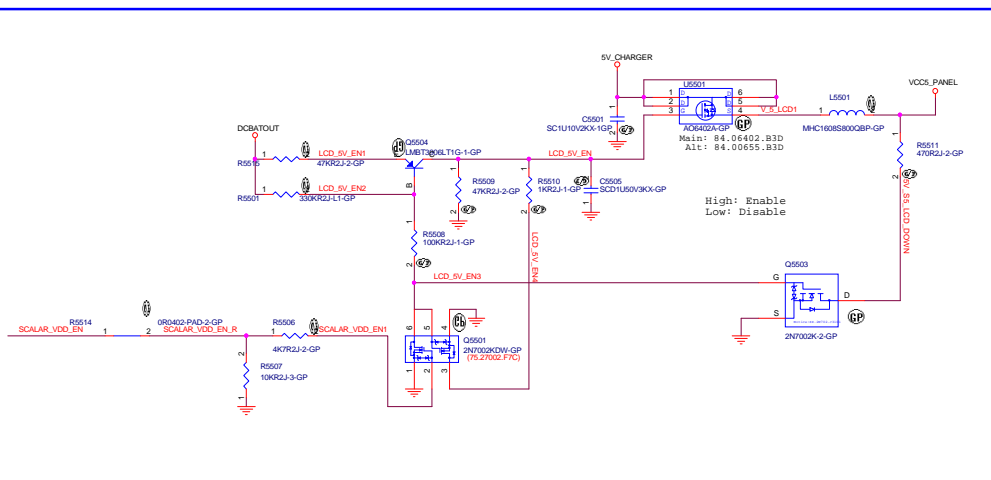
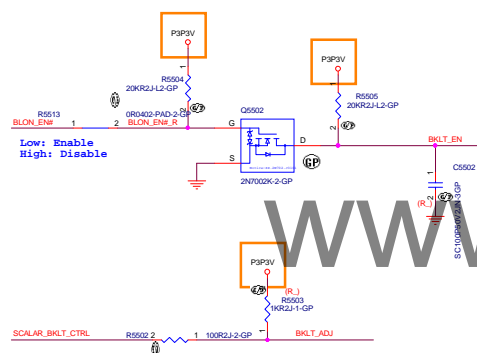
95 SCALAR_BKLT_CTRL << SCALAR_BKLT_CTRL
95 SCALAR_VDD_EN >> SCALAR_VDD_EN

```

95 BLON\_EN# >>> BLON\_EN#

24,44 BKLT\_EN << BKLT\_E

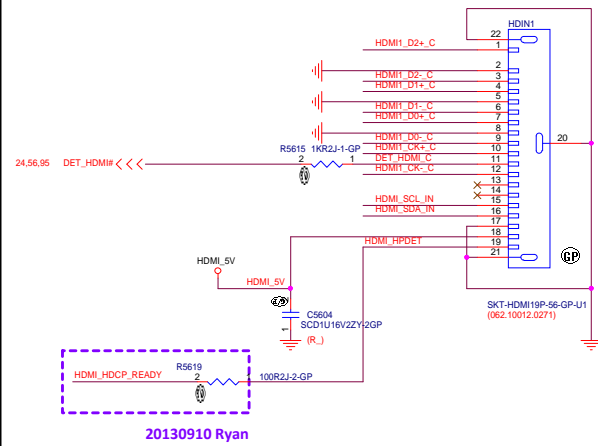
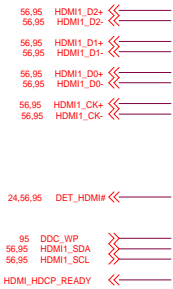
44 BKLT\_ADJ  $\ll \frac{BKLT\_ADJ}{2}$



## HDMI-IN

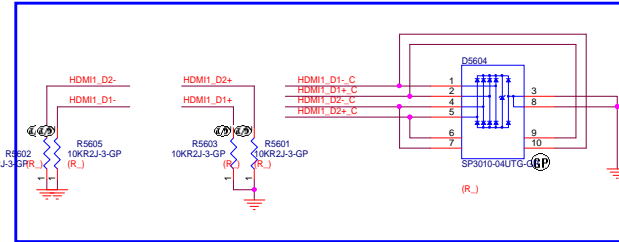
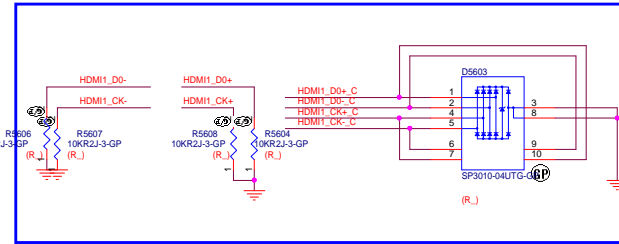
## Connector

### HDMI

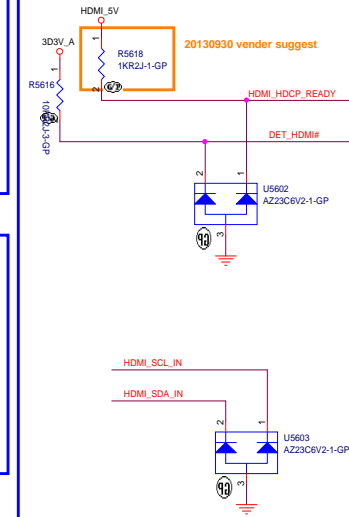


20130910 Ryan

## EMI/ESD near Connector



## EMI/ESD near Connector

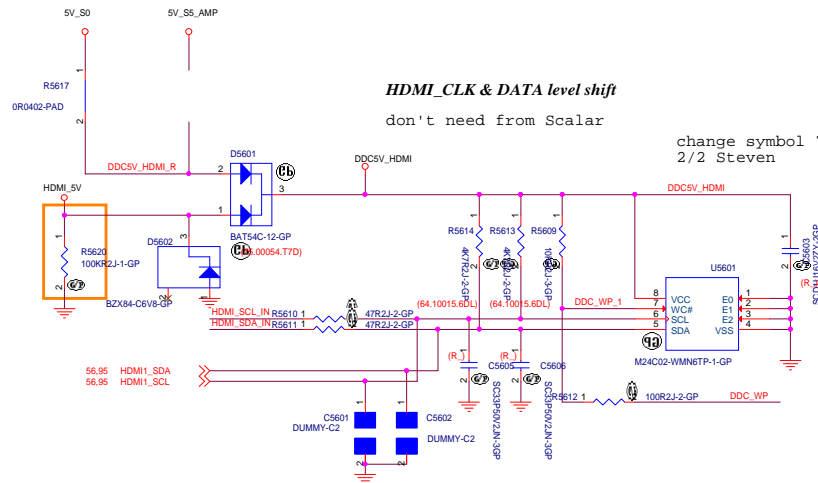


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## HDMI\_CLK & DATA level shift

don't need from Scalar

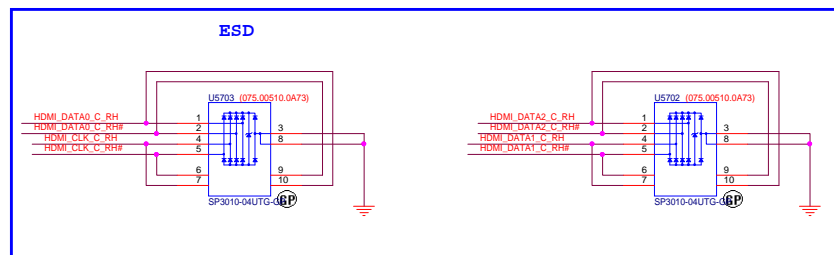
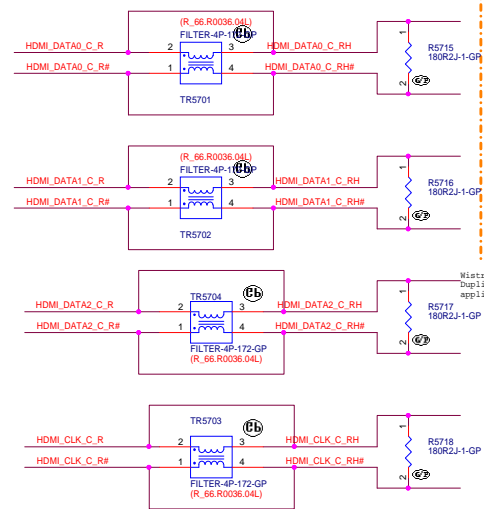
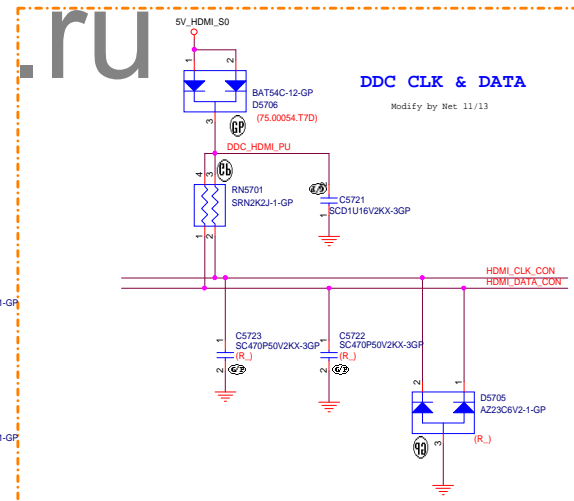
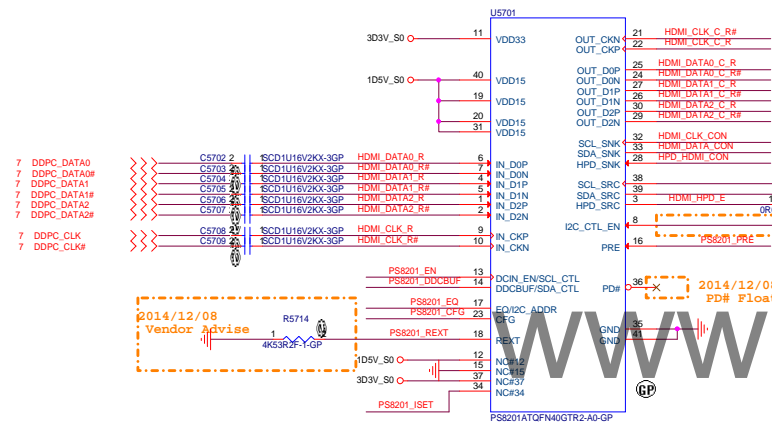
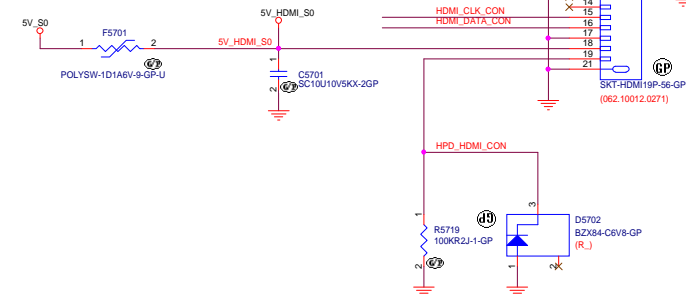
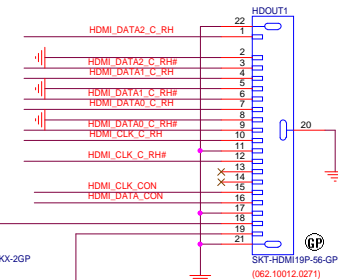
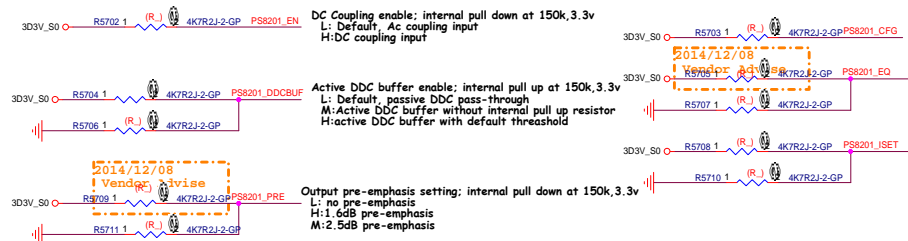
change symbol 72.02402.F01 to 72.24C02.0C1  
 2/2 Steven



SSID = VIDEO

## HDMI Level Shifter & CONNECTOR

Follow Scotland

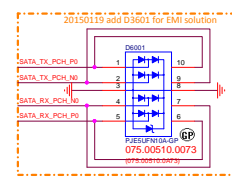
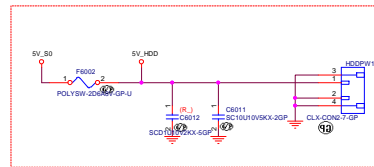
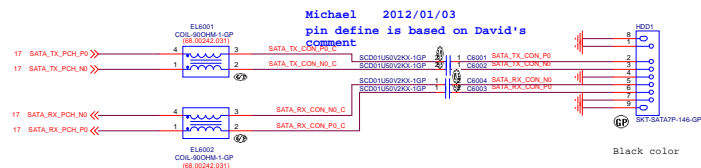


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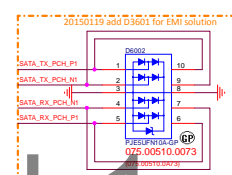
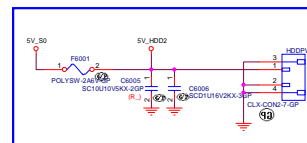
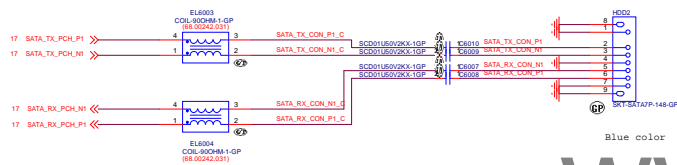
Reserved  
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# SATA Port 0 SATA HDD Connector



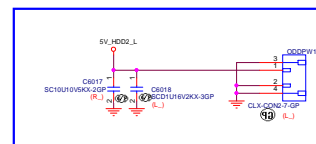
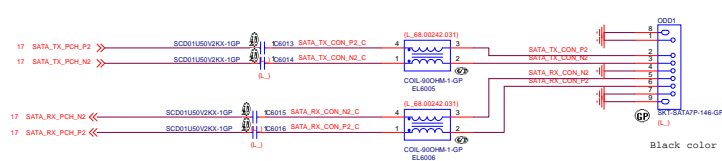
## SATA Port 1

### SATA HDD Connector

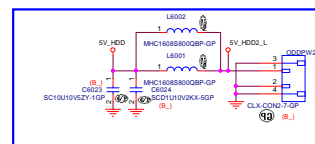
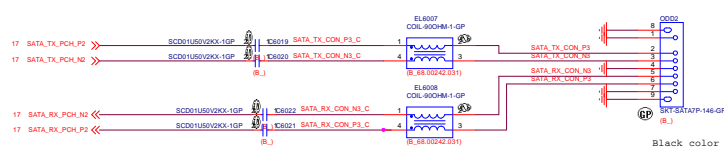


## SATA Port 2

### ODD Connector



### ODD Connector



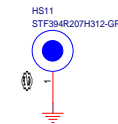
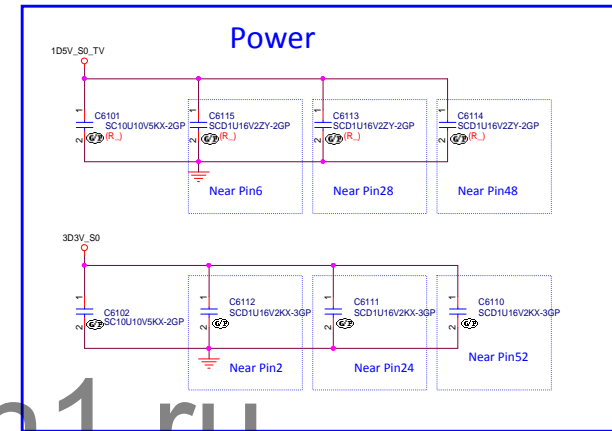
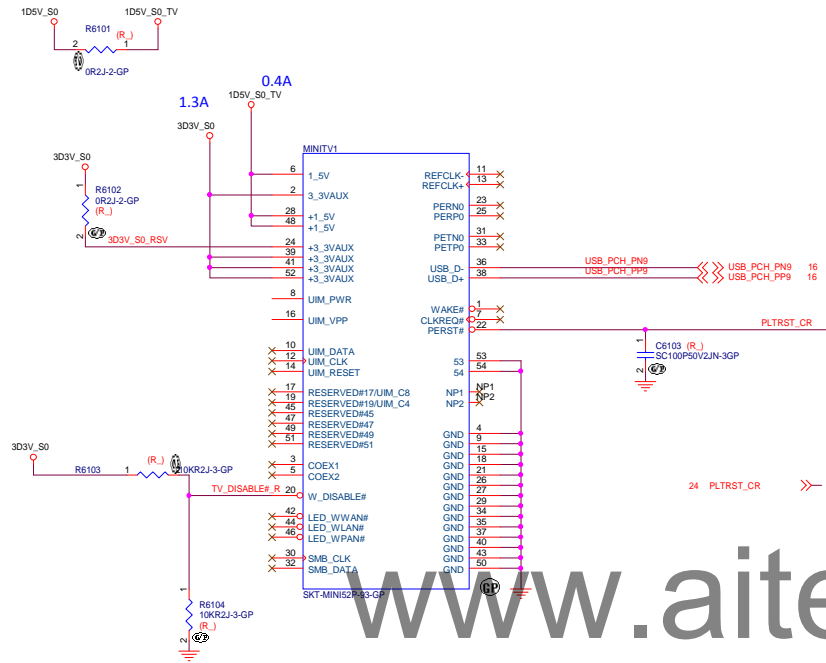
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**wistron**

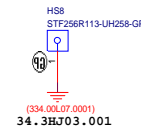
Wistron Incorporated  
21F, 88, Sec 1 Hsin Tai Wu Rd  
Hsinchu, Taipei Hsin

Doc: HDD000D  
Consumer AIO Scotland  
Date: Friday, August 21, 2015 Sheet: 60 of 107

## Mini Card Connector (TV Tuner)



FOR LOCK TV CARD.



|    |             |   |
|----|-------------|---|
| 16 | USB_PCH_PP6 |  |
| 16 | USB_PCH_PN6 |  |

```

16 PCIE_RX_PCH_N7
16 PCIE_RX_PCH_P7
16 PCIE_TX_WLAN_N7
16 PCIE_TX_WLAN_P7

18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#

```

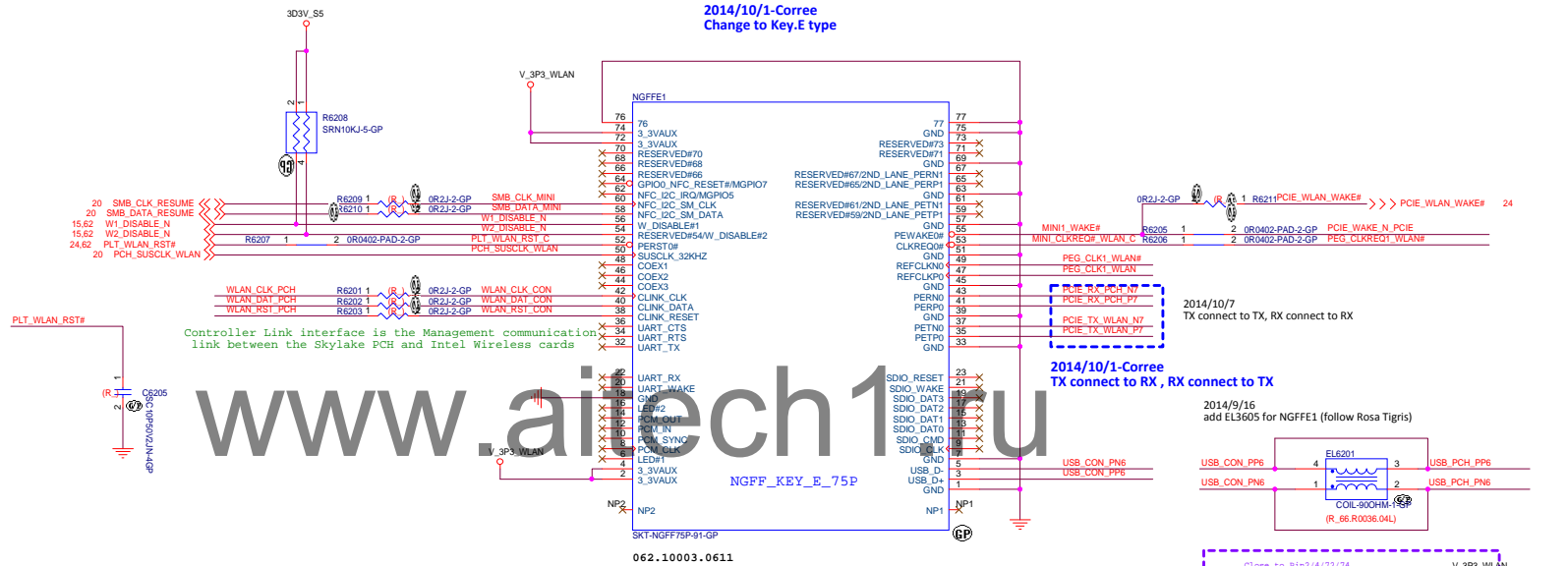
|       |                   |     |
|-------|-------------------|-----|
| 20    | PCIE_WAKE_N_PCIE  | <<— |
| 24,62 | PLT_WLAN_RST#     | >>— |
| 18    | PEG_CLKREQ1_WLAN# | <<— |
| 15,62 | W1_DISABLE_N      | >>— |
| 15,62 | W2_DISABLE_N      | >>— |

```

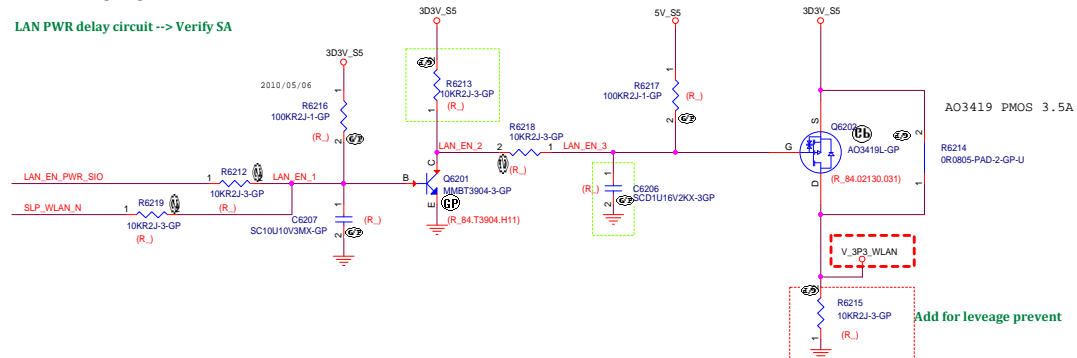
20  SLP_WLAN_N    >> SLP_WLAN_N
24  LAN_EN_PWR_SIO >> LAN_EN_PWR_SIO

```

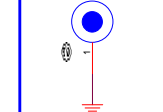
2014/10/1-Corree  
Change to Key.E type



### LAN PWR delay circuit --> Verify SA



STF256R109H124-GP

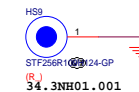
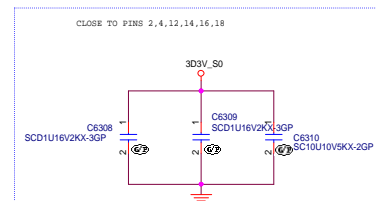
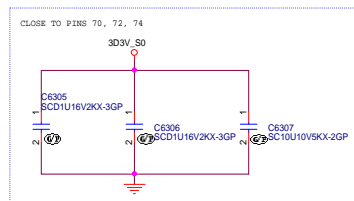


**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

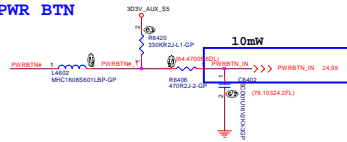
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|-------|-----------------|------------------------------|
| Title |                 | <b>WLAN and BT-NGFF</b>      |
| Size  | Document Number |                              |
| C     |                 | <b>Consumer AIO Scotland</b> |

Rev

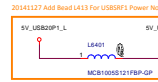
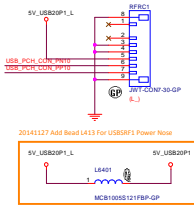
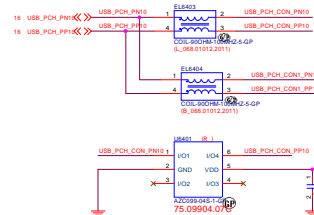
The SUSCLK pin provides a Slow Clock signal of 32 kHz to enable Low Power States.



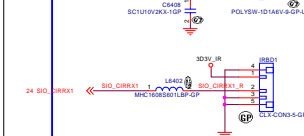
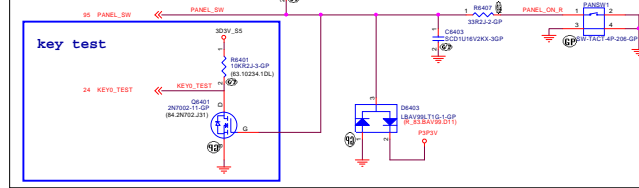
## PWR\_BTN



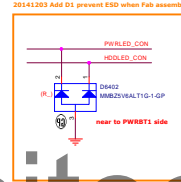
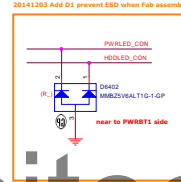
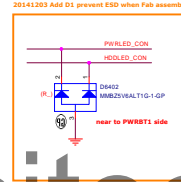
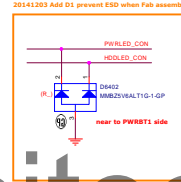
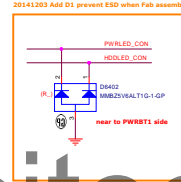
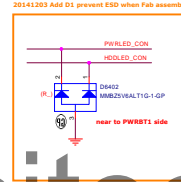
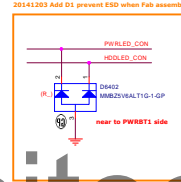
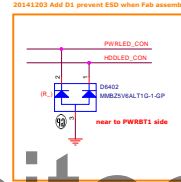
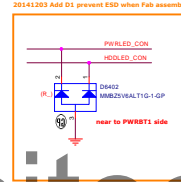
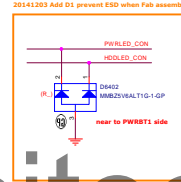
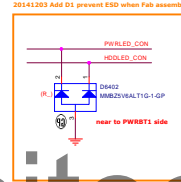
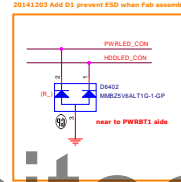
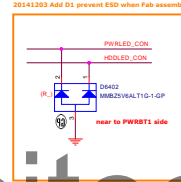
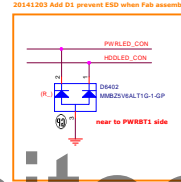
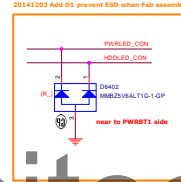
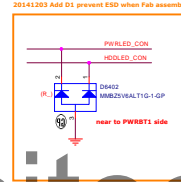
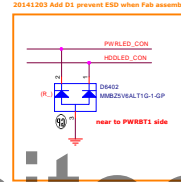
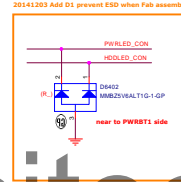
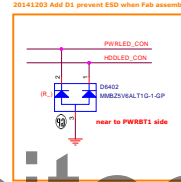
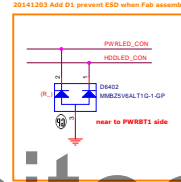
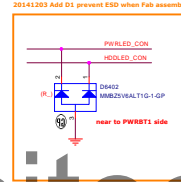
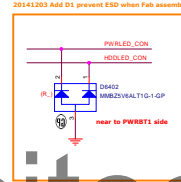
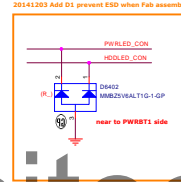
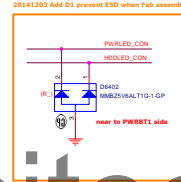
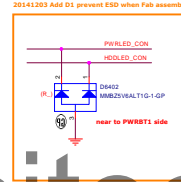
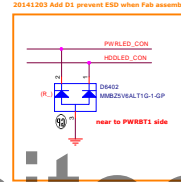
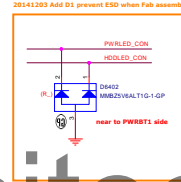
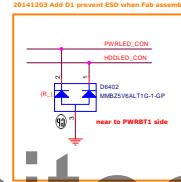
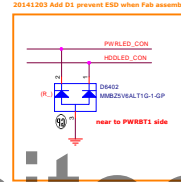
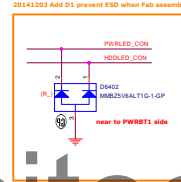
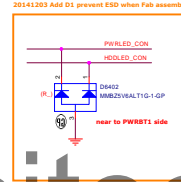
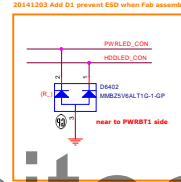
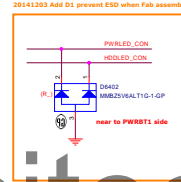
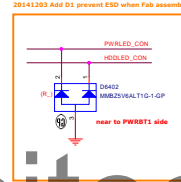
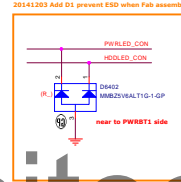
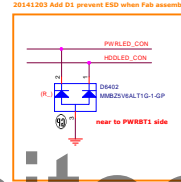
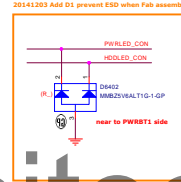
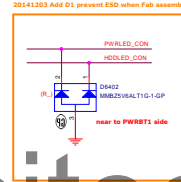
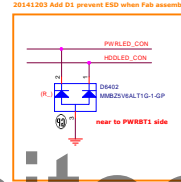
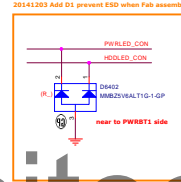
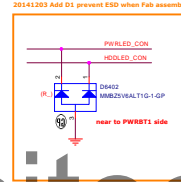
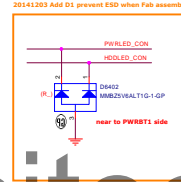
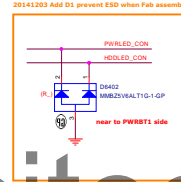
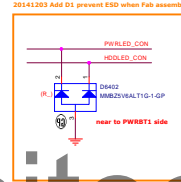
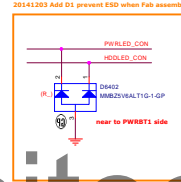
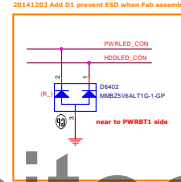
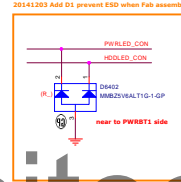
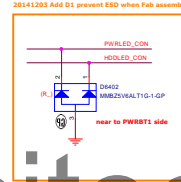
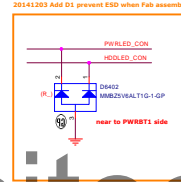
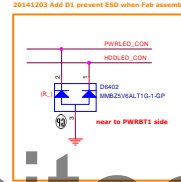
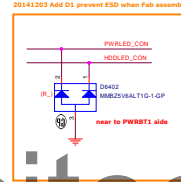
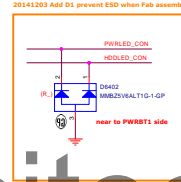
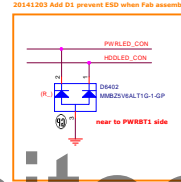
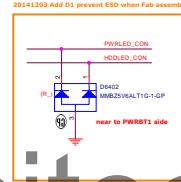
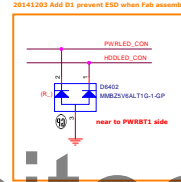
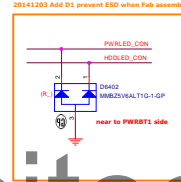
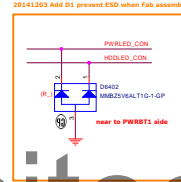
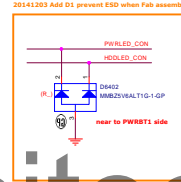
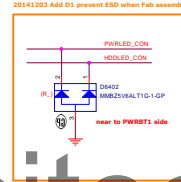
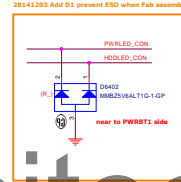
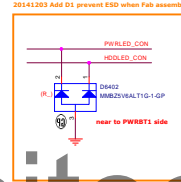
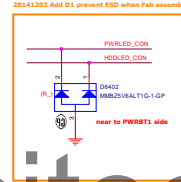
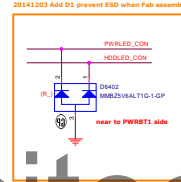
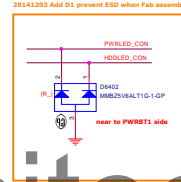
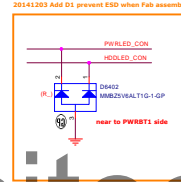
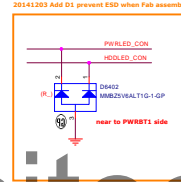
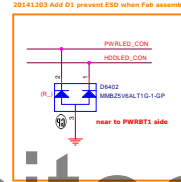
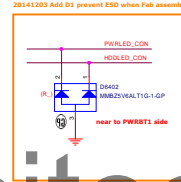
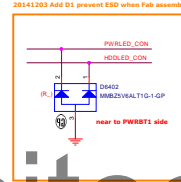
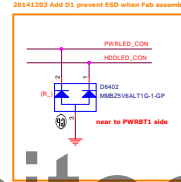
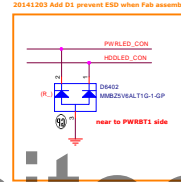
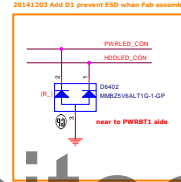
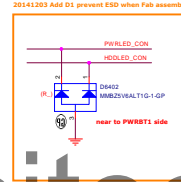
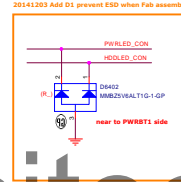
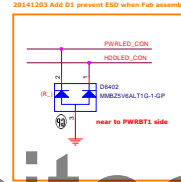
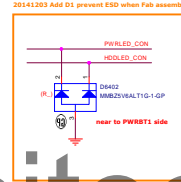
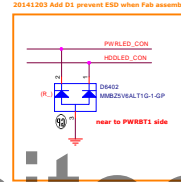
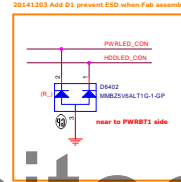
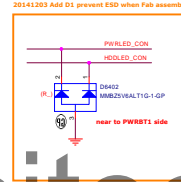
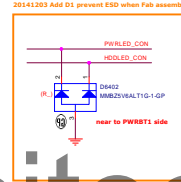
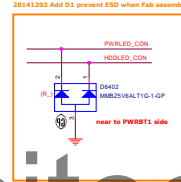
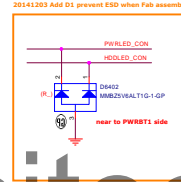
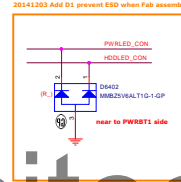
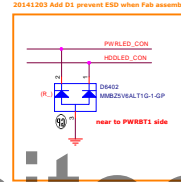
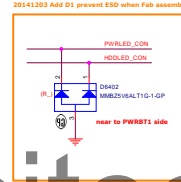
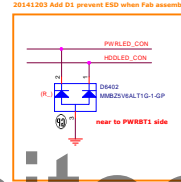
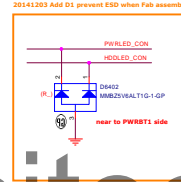
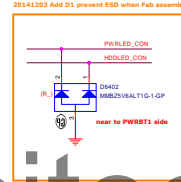
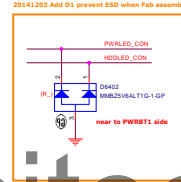
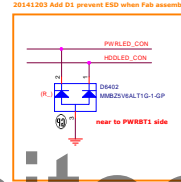
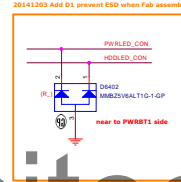
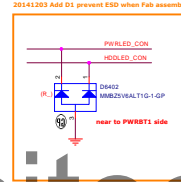
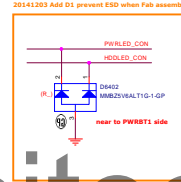
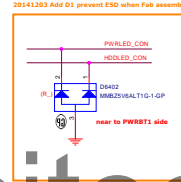
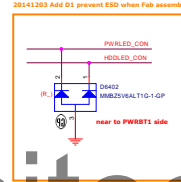
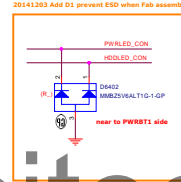
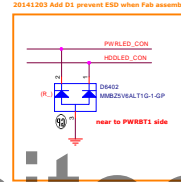
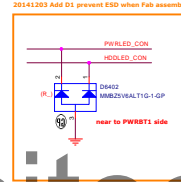
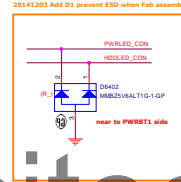
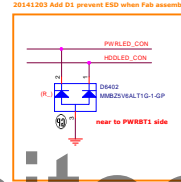
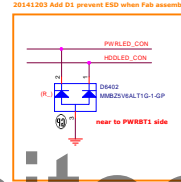
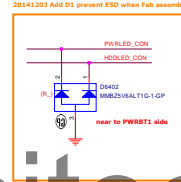
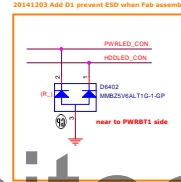
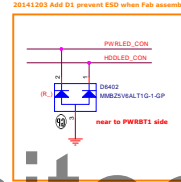
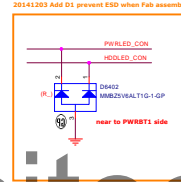
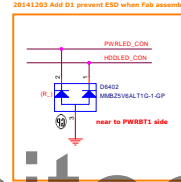
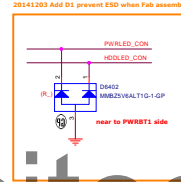
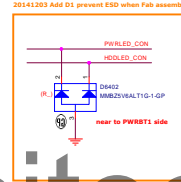
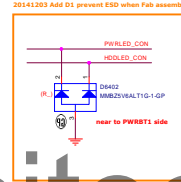
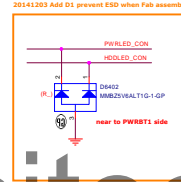
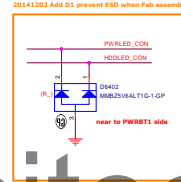
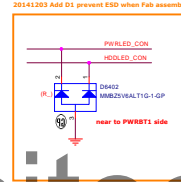
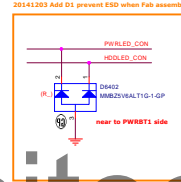
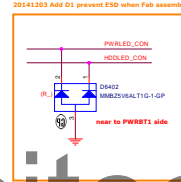
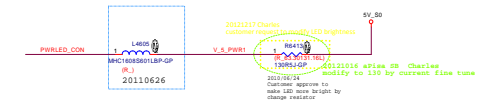
### 20141127 Ruei L412,D33 Closed PWRBT1



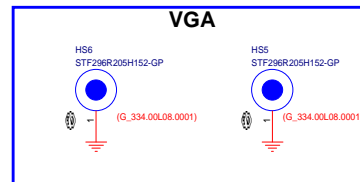
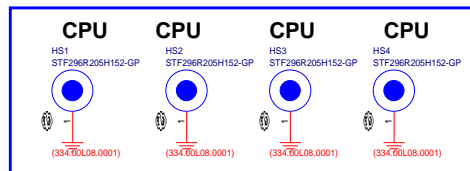
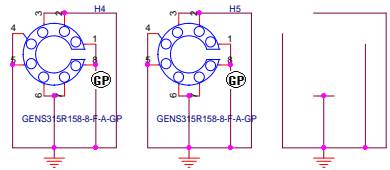
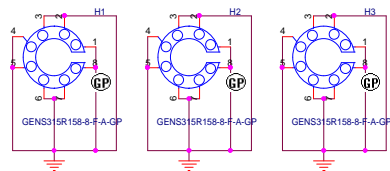
## Pannel\_SW



### 20150109 modify PWRLED behavior S0: white(keep light) S3: amber(blink)

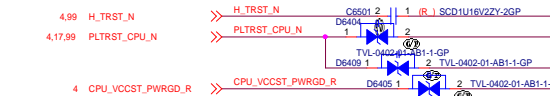


## Stand off&Hole

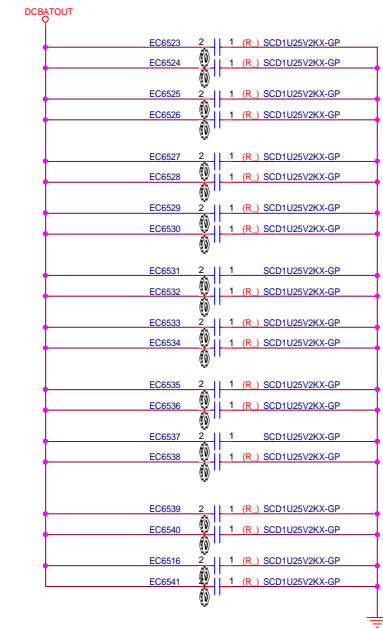
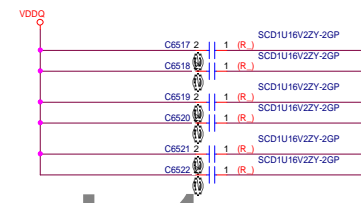
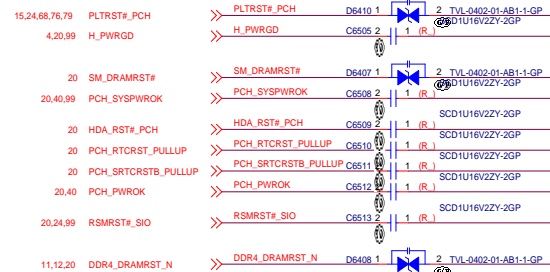


## EMI CAP

### EMI/ESD near CPU

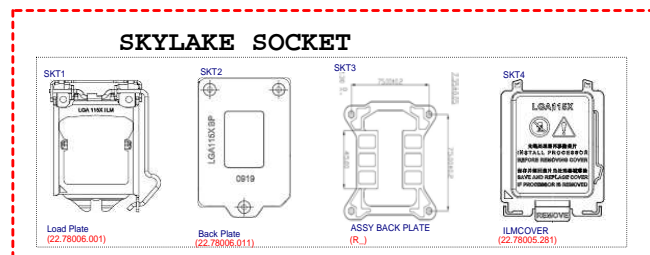


### EMI/ESD near PCH



## DUMMY BOM

### Material part



GSKT1  
GASKET  
(R\_334.03508.0001)



GSKT2  
GASKET  
(R\_334.03508.0001)

GASKET FOR WIESON HDMI

GASKET FOR TCONN HDMI

## Battery Symbol



Vendor  
P/N:  
23.20068.001  
23.20023.311  
23.22063.001



BAT2  
BATTERY BR2032\_60MM  
(R\_23.24220.612)  
Wire Length: 60mm  
耐高温>85C

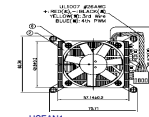
Vendor  
P/N:  
23.21208.061  
23.24220.612

## LABEL



MB serial NO# and MAC address  
40.3B224.011 -> 30 x 15mm  
40.3KP03.011 -> 35 x 15mm  
45.41107.021 -> 70 x 8mm  
CARD  
45.ACA01.0C1 -> 32 x 7mm  
MIC CARD  
345.02801.0001 -> 12 x 6mm

## HeatSink+FAN Symbol



Vendor  
P/N:

## Del PCHHS1 by Thermal--Ryan 0225

### Heatsink Symbol



PCHHS1  
HEATSINK  
(R\_30.3MN01.001)

Vendor  
P/N:  
60.3MN01.011(second source)  
60.3MN01.001



BAT1  
BATTERY CR2032\_30MM  
(L\_23.21221.024)  
Wire Length: 30mm

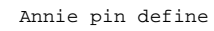
Vendor  
P/N:  
23.21221.024  
23.21212.031

|   |   |
|---|---|
| <b>wistron</b><br>Wistron Incorporated<br>21F, 88, Sec.1, Hsin Tai Wu Rd<br>Hsinchu, Taipei, Taiwan |   |
| Title<br><b>Stand off&amp;EMI Cap&amp;DUMMY BOM</b>   |   |
| Size<br>C   | Document Number<br><b>Consumer AIO Scotland</b> |
| Date<br>Wednesday, August 26, 2015  | Sheet<br>65 of 107                              |

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Layout close to SIO



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<Core Design>



**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

|        |                         |  |         |                 |
|--------|-------------------------|--|---------|-----------------|
| Title  |                         |  | LPT_(R) |                 |
| Size   | Document Number         |  |         | Rev             |
| Custom | Consumer AIO Scotland   |  |         | SA              |
| Date:  | Friday, August 21, 2015 |  |         | Sheet 69 of 107 |

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|  |   |
|--|---|
| <Core Design>  |   |
|  <b>Wistron Incorporated</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd<br>Hsichih, Taipei Hsien |   |
| Title<br><b>Thunderbolt (R)</b>  |   |
| Size<br>C  | Document Number<br><b>Consumer AIO Scotland</b> |
| Date:<br>Friday, August 21, 2015   | Rev<br>SA                                       |
| Sheet 73 of 107  |   |

Reserved

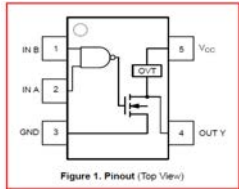
www.aitech1.ru

|  |   |
|--|---|
| <Core Design>  |   |
|  <b>Wistron Incorporated</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd<br>Hsichih, Taipei Hsien |   |
| Title<br><b>Thunderbolt (R)</b>  |   |
| Size<br>C  | Document Number<br><b>Consumer AIO Scotland</b> |
| Date:<br>Friday, August 21, 2015   | Rev<br>SA                                       |
| Sheet 74 of 107  |   |

Reserved  
www.aitech1.ru

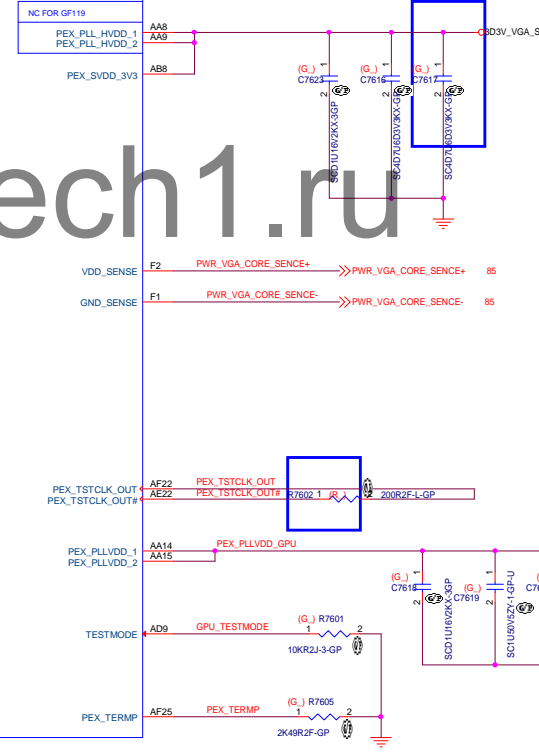
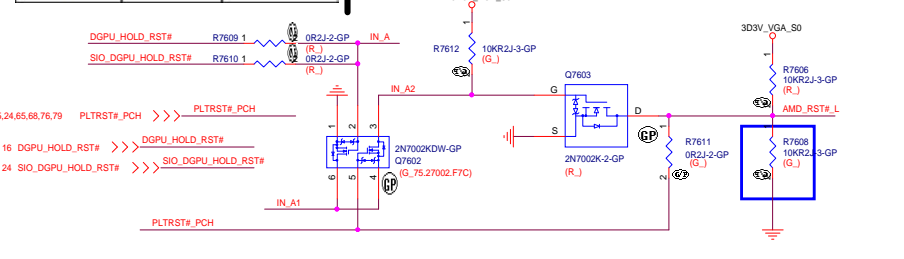
# PCIE X8

3 PEG\_TX\_CPU\_P0[0..7] >>> PEG\_TX\_CPU\_N0[0..7]  
 3 PEG\_RX\_CPU\_P0[0..7] >>> PEG\_RX\_CPU\_N0[0..7]  
 18,76 PEG\_CLK8\_PCH >>> PEG\_CLK8\_PCH#  
 18,76 PEG\_CLK8\_PCH# >>> PLTRST#\_PCH  
 15,24,65,68,76,79 PLTRST#\_PCH >>> PEG\_RST\_GPU



## FUNCTION TABLE

| Input |   | Output<br>Y = AB |
|-------|---|------------------|
| A     | B | Y                |
| L     | L | L                |
| L     | H | L                |
| H     | L | L                |
| H     | H | H                |



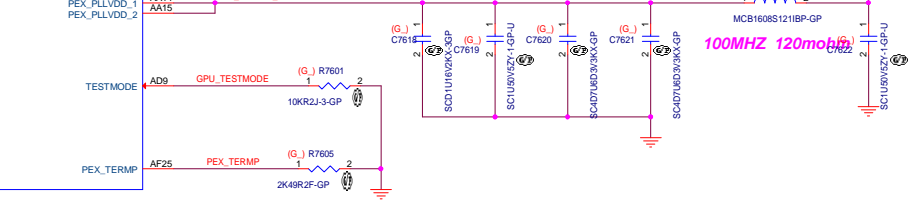
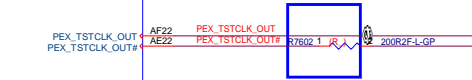
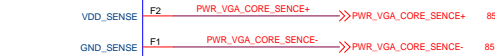
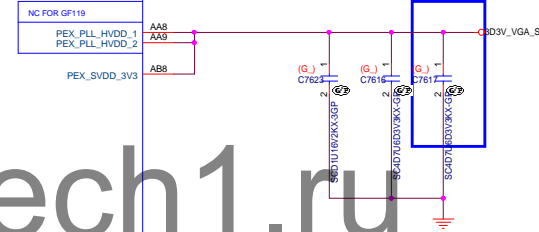
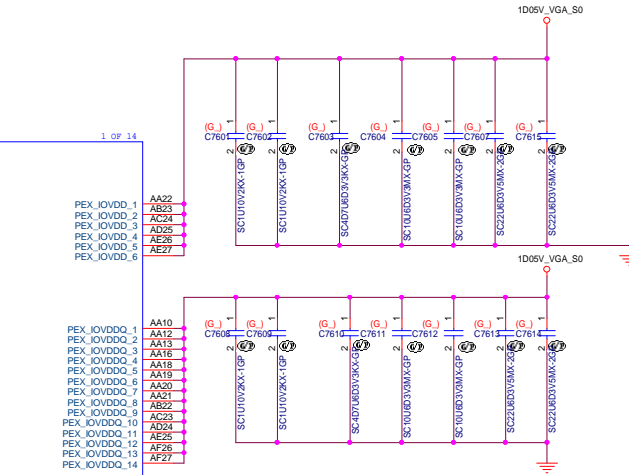
1U Under GPU

4.7U NEAR TO GPU

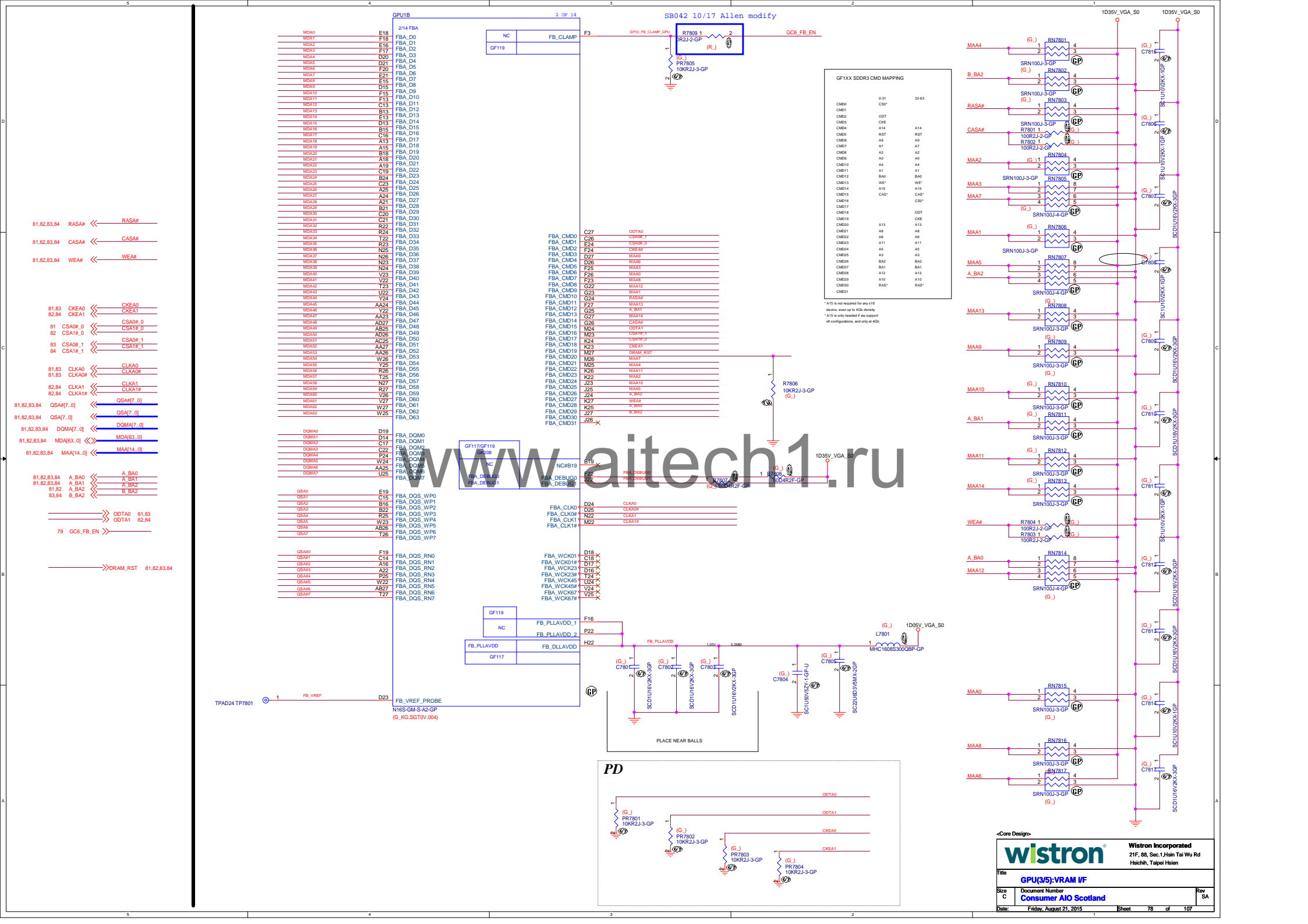
10U mid TO GPU

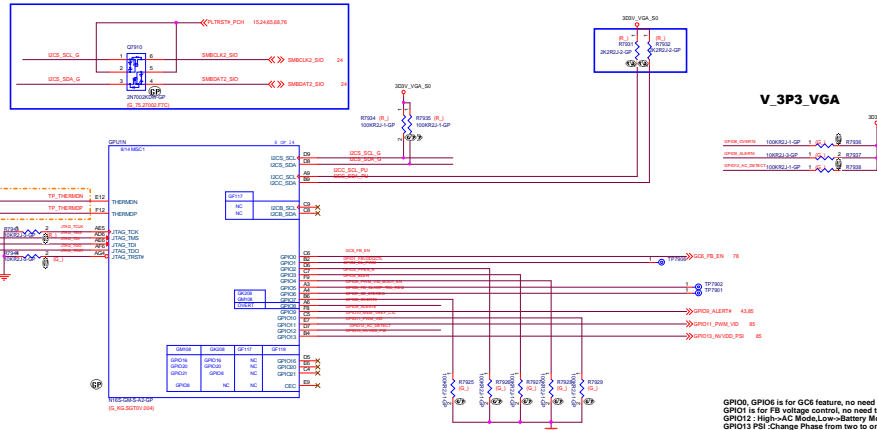
Michael 2011/12/12

Add two 1uF Caps according to the NV Comment









| GPIO   | GF117                              |
|--------|------------------------------------|
| GPIO0  | FAIL, PWRM, CLAMP, DEBURG Service  |
| GPIO1  | MEM_VDD_CTL                        |
| GPIO2  | UNUSED                             |
| GPIO3  | UNUSED                             |
| GPIO4  | UNUSED                             |
| GPIO5  | Reserved                           |
| GPIO6  | FB_CLAMP_TOL_REQ                   |
| GPIO7  | 3D Vision (AUXES)                  |
| GPIO8  | GPU Overtemp                       |
| GPIO9  | GPU Thermal Alert                  |
| GPIO10 | FB Vref Control                    |
| GPIO11 | MVDDO PWRM_VDD                     |
| GPIO12 | UNUSED (Only Used to Set in VDDIO) |
| GPIO13 | PWRM Level AC Direct               |
| GPIO14 | UNUSED (Only Used to Set in VDDIO) |
| GPIO15 | NA on Package                      |
| GPIO16 | NA on Package                      |
| GPIO17 | NA on Package                      |
| GPIO18 | NA on Package                      |
| GPIO19 | NA on Package                      |
| GPIO20 | NA on Package                      |
| GPIO21 | NA on Package                      |

Table 115. GB2-64 and GB4-128 GPIO Description

| Pin    | Normal Function  | I/O | Functional Description              | Recommended Default Pull-up or Pull-down |
|--------|------------------|-----|-------------------------------------|--|
| GPIO0  | FB_CLAMP_REQ     | I   | FB Clamp monitor                    | 100 K pull-up                            |
| GPIO1  | MEM_VDD_CTL      | O   | Memory VDD Strap to boot            | 100 K pull-down                          |
| GPIO2  | LCED_B_PWM       | O   | Power Backlight Pulse               | 100 K pull-down                          |
| GPIO3  | LCED_VCC         | O   | Power Backlight Enable              | 100 K pull-down                          |
| GPIO4  | LCED_B_PWM       | O   | Power Backlight Enable              | 100 K pull-down                          |
| GPIO5  | Reserved         |     |                                     |  |
| GPIO6  | FB_CLAMP_TOL_REQ | O   | Active low FB Clamp toggle request  | 100 K pull-up                            |
| GPIO7  | 3D Vision        | I   | 3D Vision L/R signal                | 100 K pull-down                          |
| GPIO8  | CHERT            | I/O | Active Low Thermal Calibration Over | 100 K pull-up                            |
| GPIO9  | ALERT            | I/O | Active Low Thermal Alert            | 100 K pull-up                            |
| GPIO10 | MEM_VREF_CTL     | O   | Memory VREF Control                 | 100 K pull-down                          |
| GPIO11 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO12 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO13 | PSI              | O   | Power Saving                        | 100 K pull-up                            |
| GPIO14 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO15 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO16 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO17 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO18 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO19 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO20 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |
| GPIO21 | PHOTON           | I   | GPU Lane 100 Mbps Control           | 100 K pull-up                            |

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.  
 GPIO1 is for FB voltage control, no need to connect since the FBVDD is 1.5V for all P-Sizes.  
 GPIO12 - High-AC Mode Low-Battery Mode enter slow down functional for power saving. Recommend Pull-High for AC mode.  
 GPIO13 PSI Change Phase from two to one, and then enter slow down functional for power saving.

## STRAP

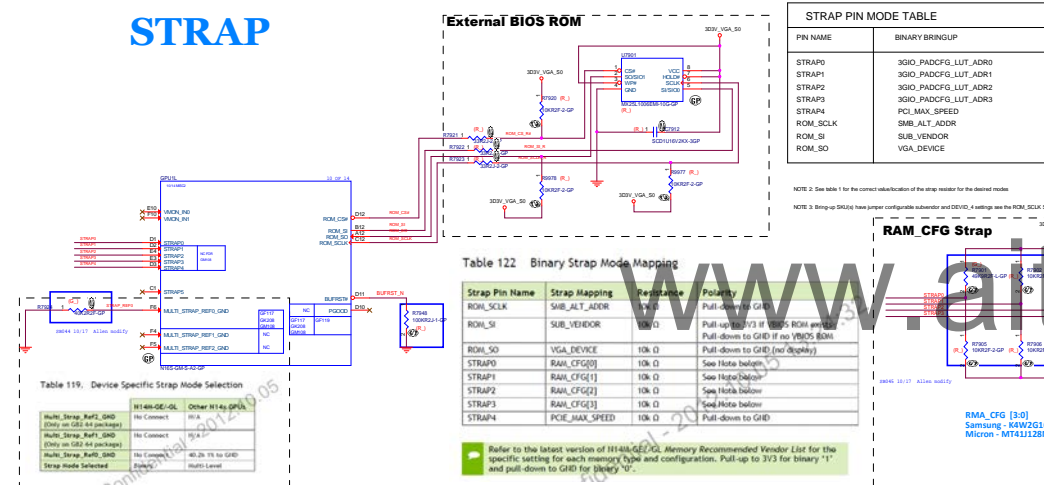
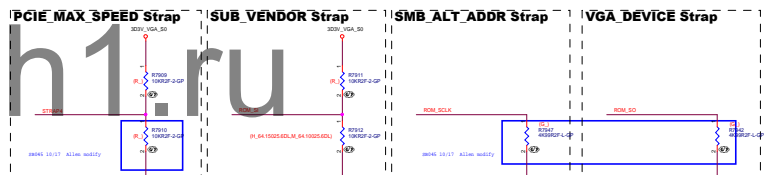
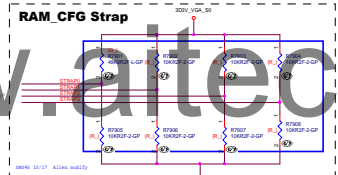


Table 1. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

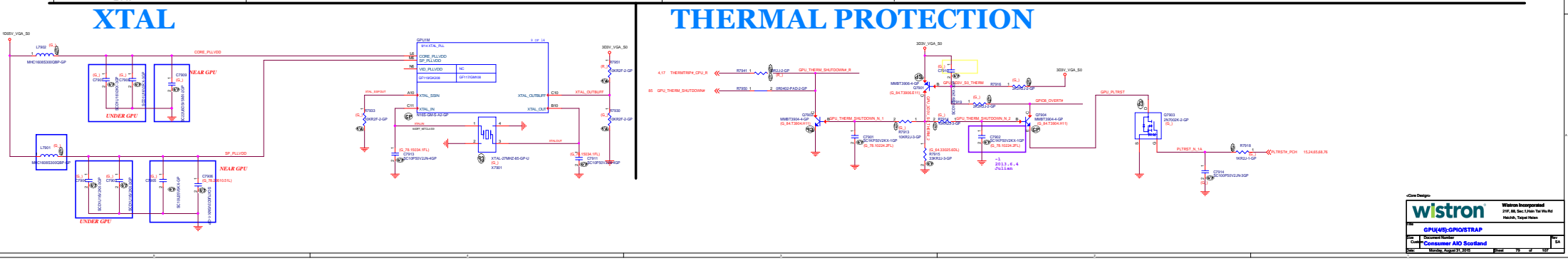
| Configuration | Vendor  | Strap | FBVDD/ FBVDDQ | Manufacturer Part Number | Max Speed CLK (MHz) | Memory Date Code Minimum | Status           |
|---------------|---------|-------|---------------|--------------------------|---------------------|--------------------------|------------------|
| 128Mx16 DDR3  | Micron  | 0x1   | 1.5 V / 1.5 V | MT41J128M16JT-093G-K     | 1000                | 1234                     | Production ready |
|               | Samsung | 0x5   | 1.5 V / 1.5 V | K4W2G1646E-BC1A          | 1000                | 1204                     | Production ready |
|               | Hynix   | 0xC   | 1.5 V / 1.5 V | H5TC2G63PFR-11C          | 1000                | N/A                      | Production ready |

Table 122 Binary Strap Mode Mapping

| Strap Pin Name | Strap Mapping  | Resistance | Polarity   |
|----------------|----------------|------------|--|
| ROM_SCLK       | SMB_ALT_ADDR   | 10K (0)    | Pull-down to GND   |
| ROM_SI         | SMB_VENDOR     | 10K (0)    | Pull-up to V3 if VDD3 ROM is not connected. Pull-down to GND if no VDD3 ROM. |
| ROM_SO         | VGA_DEVICE     | 10K (0)    | Pull-down to GND (not display)   |
| STRAP0         | RAM_CFG[0]     | 10K (0)    | See Note below   |
| STRAP1         | RAM_CFG[1]     | 10K (0)    | See Note below   |
| STRAP2         | RAM_CFG[2]     | 10K (0)    | See Note below   |
| STRAP3         | RAM_CFG[3]     | 10K (0)    | See Note below   |
| STRAP4         | PCIE_MAX_SPEED | 10K (0)    | Pull-down to GND   |



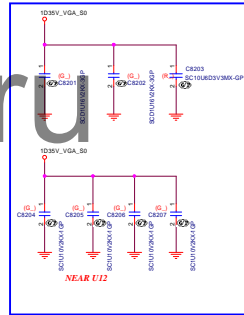
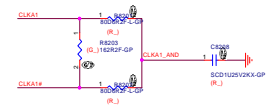
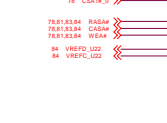
## THERMAL PROTECTION



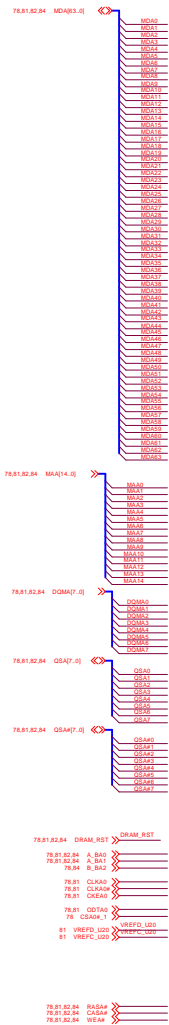




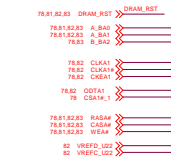
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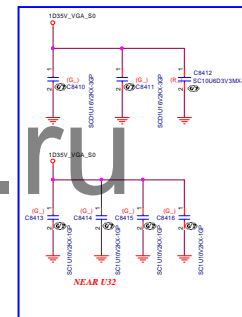
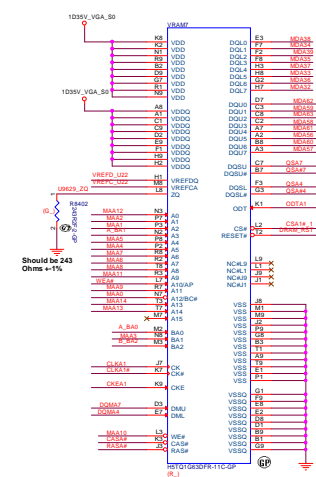
# CHANNEL A:1GB DDR3



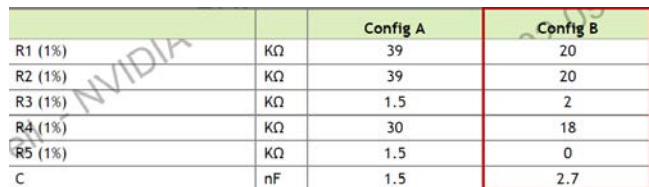
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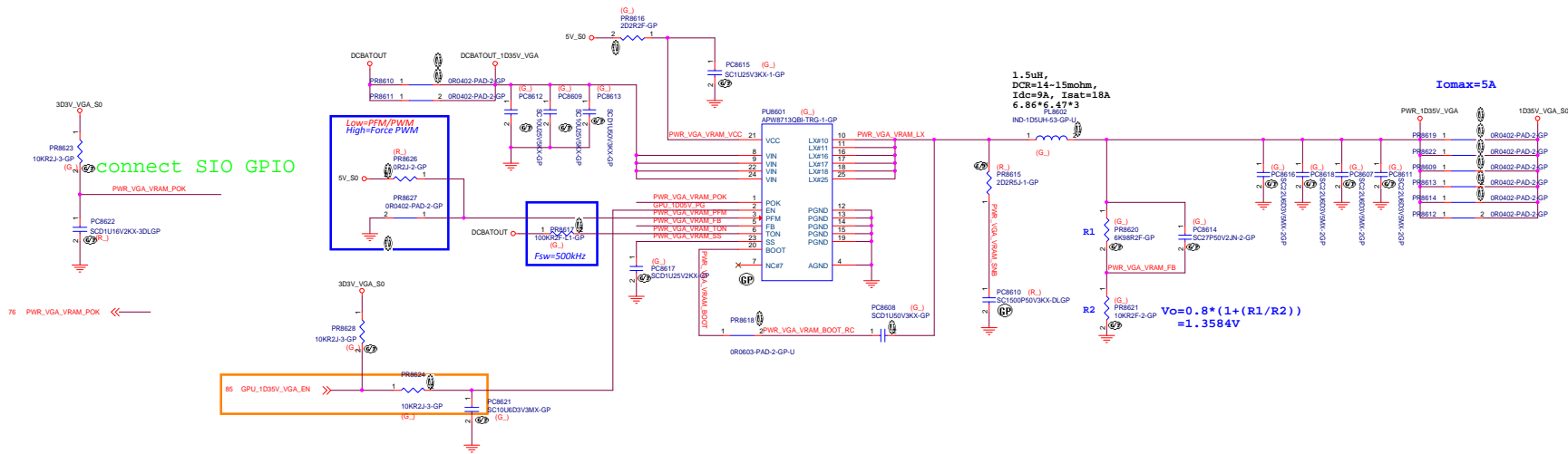
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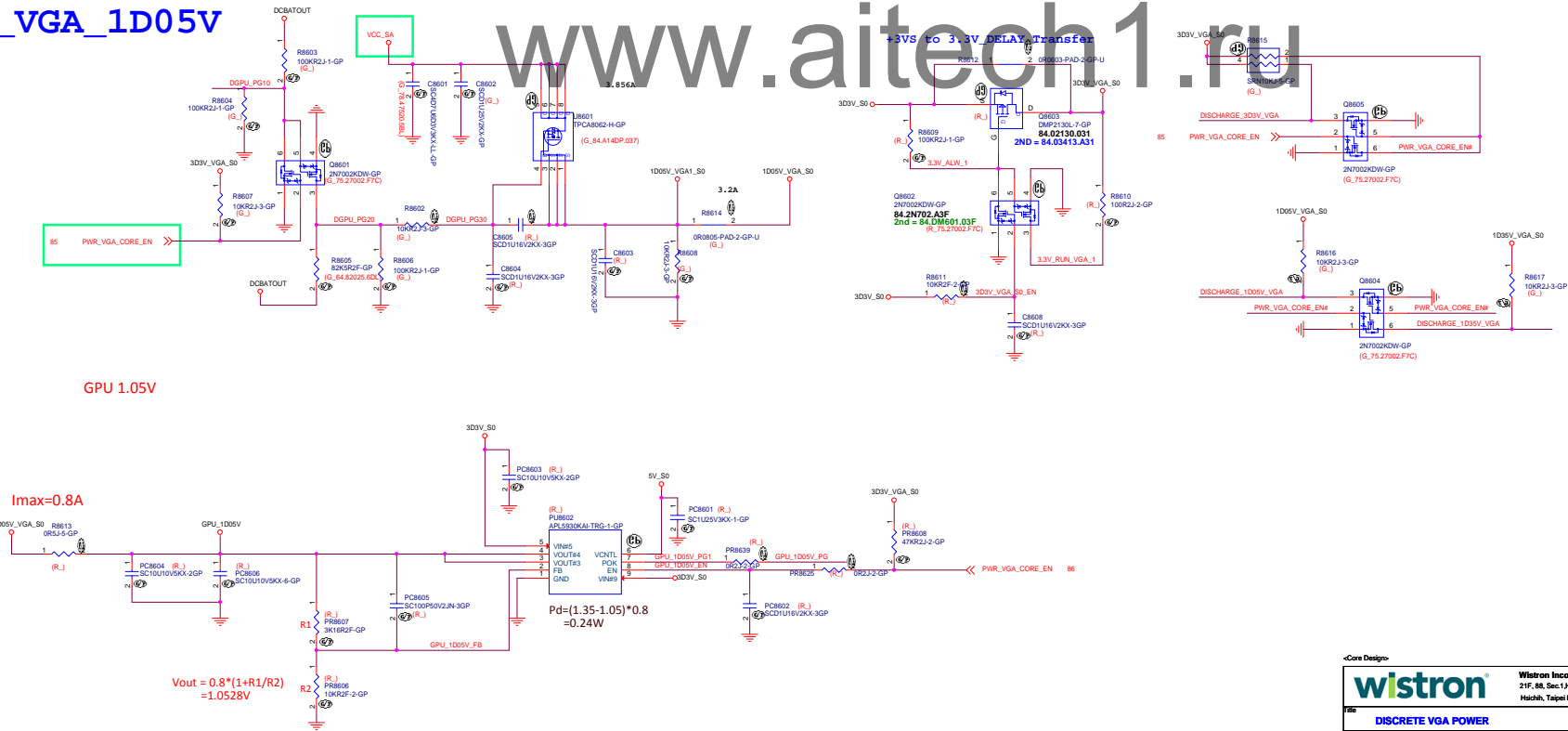
SB033 10/09 Allen remove



PWR VGA 1D35V



PWR\_VGA\_1D05V



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| Title<br>TPM_(R)  |  |   |                 |
| Size<br>Custom  | Document Number<br>Consumer AIO Scotland |   | Rev<br>SA       |
| Date:   | Friday, August 21, 2015                  |   | Sheet 91 of 107 |

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SSID = Scalar

Audio Out

18 SCALAR\_OUT\_A\_0

19 SCALAR\_OUT\_A\_1

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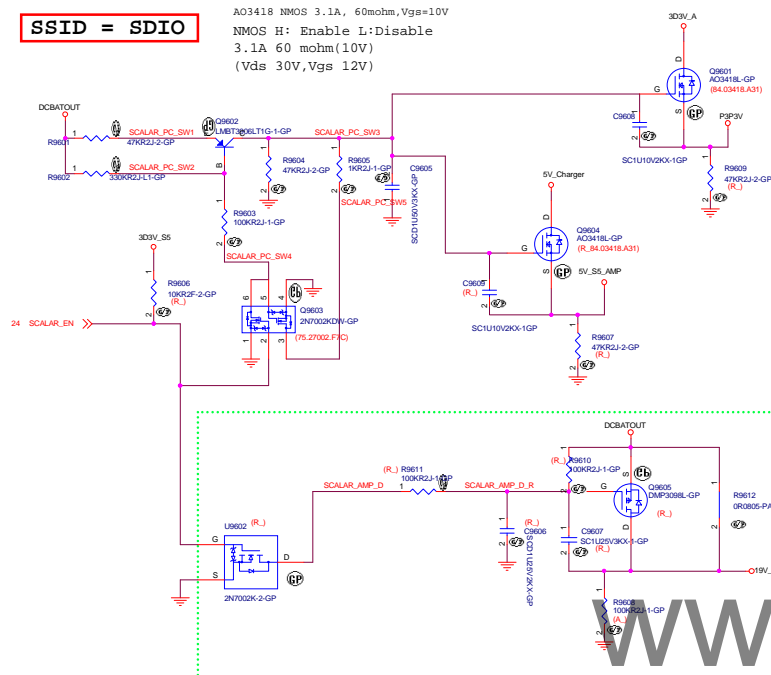
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305 SCALAR\_OUT\_A\_287

**SSID = SDIO**

AO3418 NMOS 3.1A, 60mohm,Vgs=10V  
NMOS H: Enable L:Disable  
3.1A 60 mohm(10V)  
(Vds 30V,Vgs 12V)

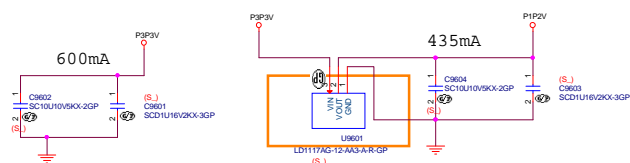


### Scalar Spec Table

| GPI input |  | From | High   | Low     | Default  |
|-----------|--|------|--------|---------|--|
| Pin69     | GPI-1 PC Power ON  PM_SLP_S3# 20,34,40,41,48,50,54,95 | SB   | PC     | Monitor | Monitor  |
| Pin109    | GPI-2 Mode change/<br>Panel OnOff  | SW   | Normal | Touch   | PC: PC (PC->HDMI)<br>Monitor: HDMI, VGA (HDMI) |

**GPO output**

|        |                    |                     |        |         |         |                                  |
|--------|--------------------|---------------------|--------|---------|---------|----------------------------------|
| Pin55  | GPO-2 Panel On/OFF | SCALAR_VDO_EN 55.95 | Scalar | ON      | OFF     | PC: ON<br>Monitor: Detect Signal |
| Pin104 | GPO-3 PC/Monitor   | PC_MONITOR_SW 28.95 | Scalar | PC      | Monitor | PC: PC,<br>Monitor: HDMI, VGA    |
| Pin101 | GPO-5 Video        | BLON_ENF 55.95      | Scalar | Disable | Enable  | Disable                          |




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| Title  |                         |
| LAN Switch_(R)   |                         |
| Size   | Document Number         |
| C  | Consumer AIO Scotland   |
| Date:  | Friday, August 21, 2015 |
| Sheet  | 98 of 107               |
| Rev  | SA                      |

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4 H_PREQ_N
4 H_PRDY_N
4 SKL_PCUSTB_0_DP
4 SKL_PCUSTB_0_DN
4 BPM_CPU_N0
4 BPM_CPU_N1
4 SKL_PCUSTB_1_DP
4 SKL_PCUSTB_1_DN

```

18 XDP\_CLK\_CON      

18 XDP\_CLK\_CON#      

4 CFG[0..15] &lt;&lt;—

4,20 H\_TCK  
4 H\_TDO  
4 H\_TDI  
4 H\_TMS  
4,65 H\_TRST\_N

15,22,25 SPI\_WP\_PCH << >>  
4 XDP\_PCUEDEBUG3 << >>  
21 XDP\_PRDY\_N << >>  
21 PCH\_XDP\_PREQ\_R\_N << >>

15,22,25 SPI\_SI\_PCH << >> \_\_\_\_\_

20,24,65 RSMRST#\_SIO >> \_\_\_\_\_

4,40 CPU\_VCCST\_PWRGD &gt;&gt;

24,64 PWRBTN\_IN >>

20 ITP\_PMODE >>—

20 FP\_RST\_N 

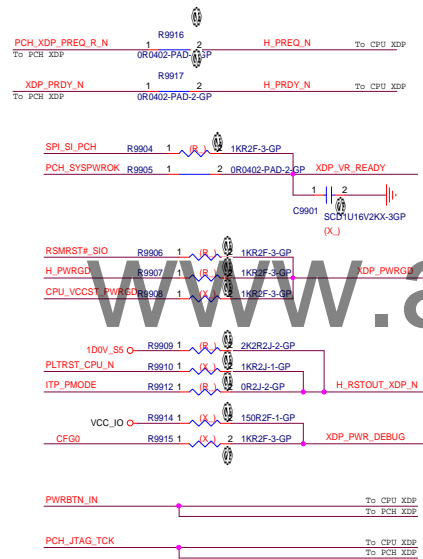
20 PCH\_JTAG\_TCK >>—

4,17,65 PLTRST\_CPU\_N >>—

4,20,65 H\_PWRGD >>

11,12,20,79,95 SMB\_DATA\_MAIN << >>—

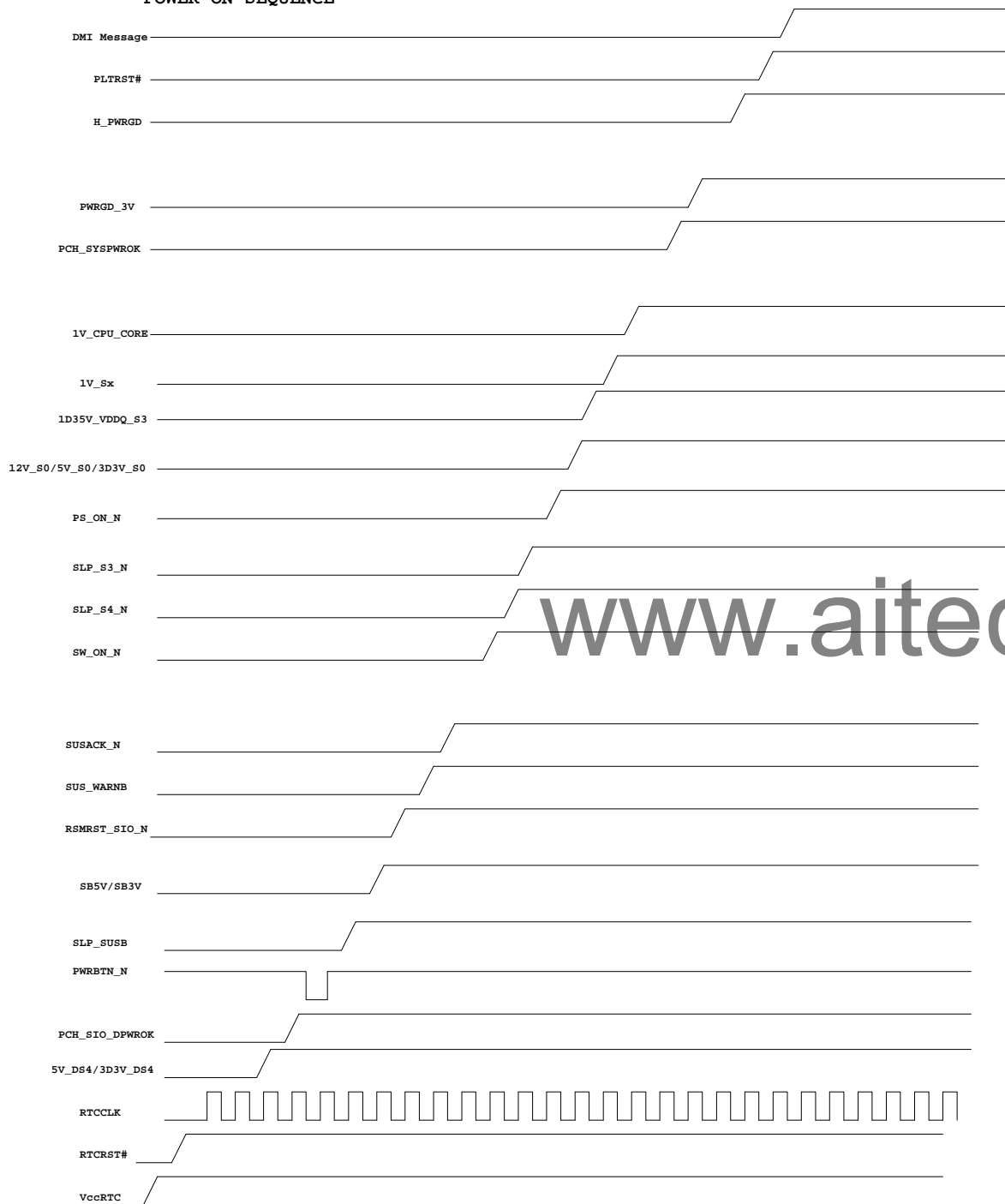
11,12,20,79,95 SMB\_CLK\_MAIN << >>—



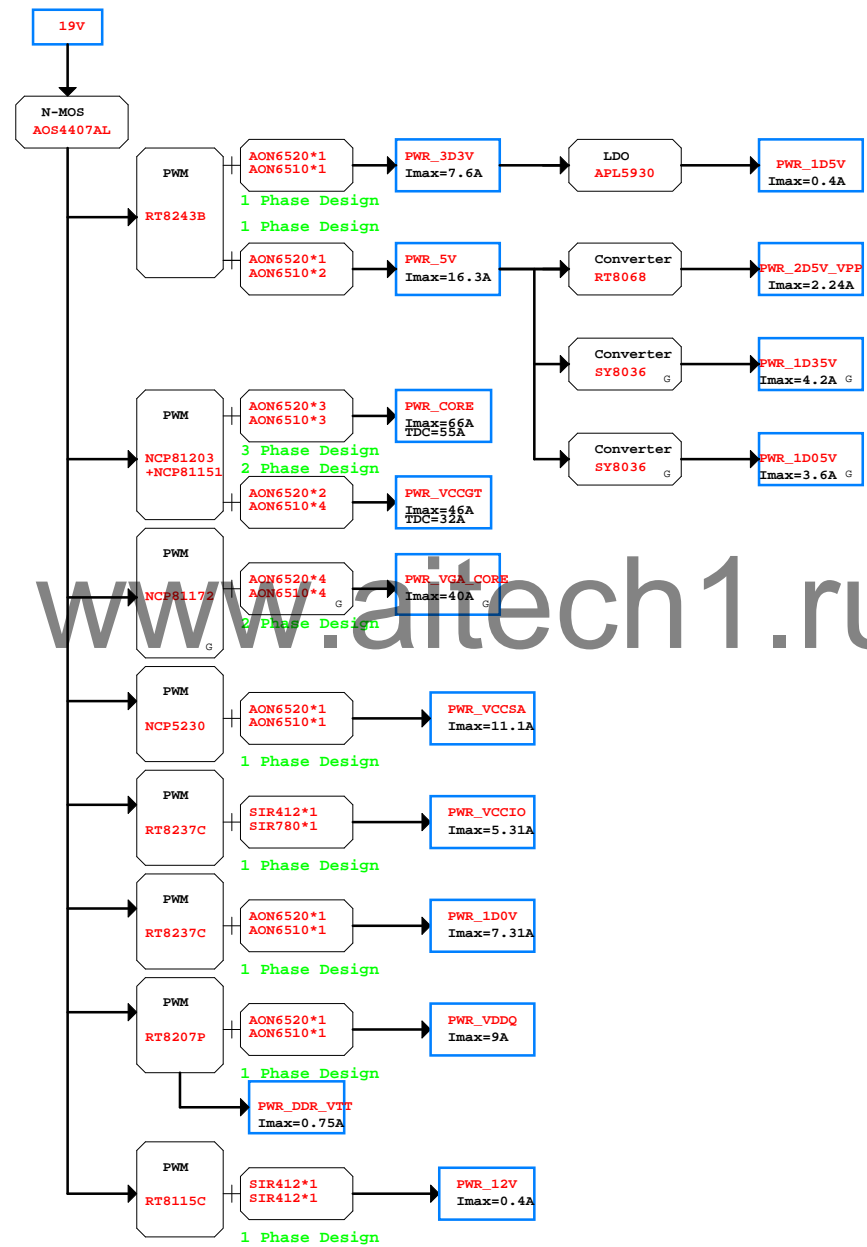
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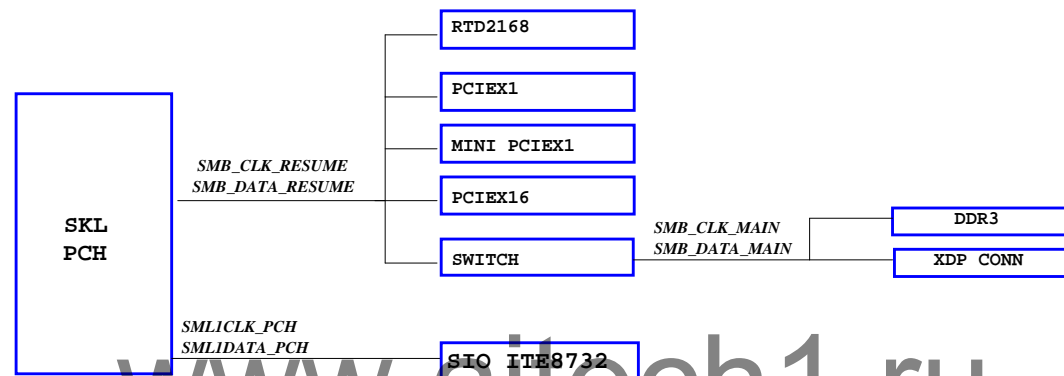
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POWER ON SEQUENCE

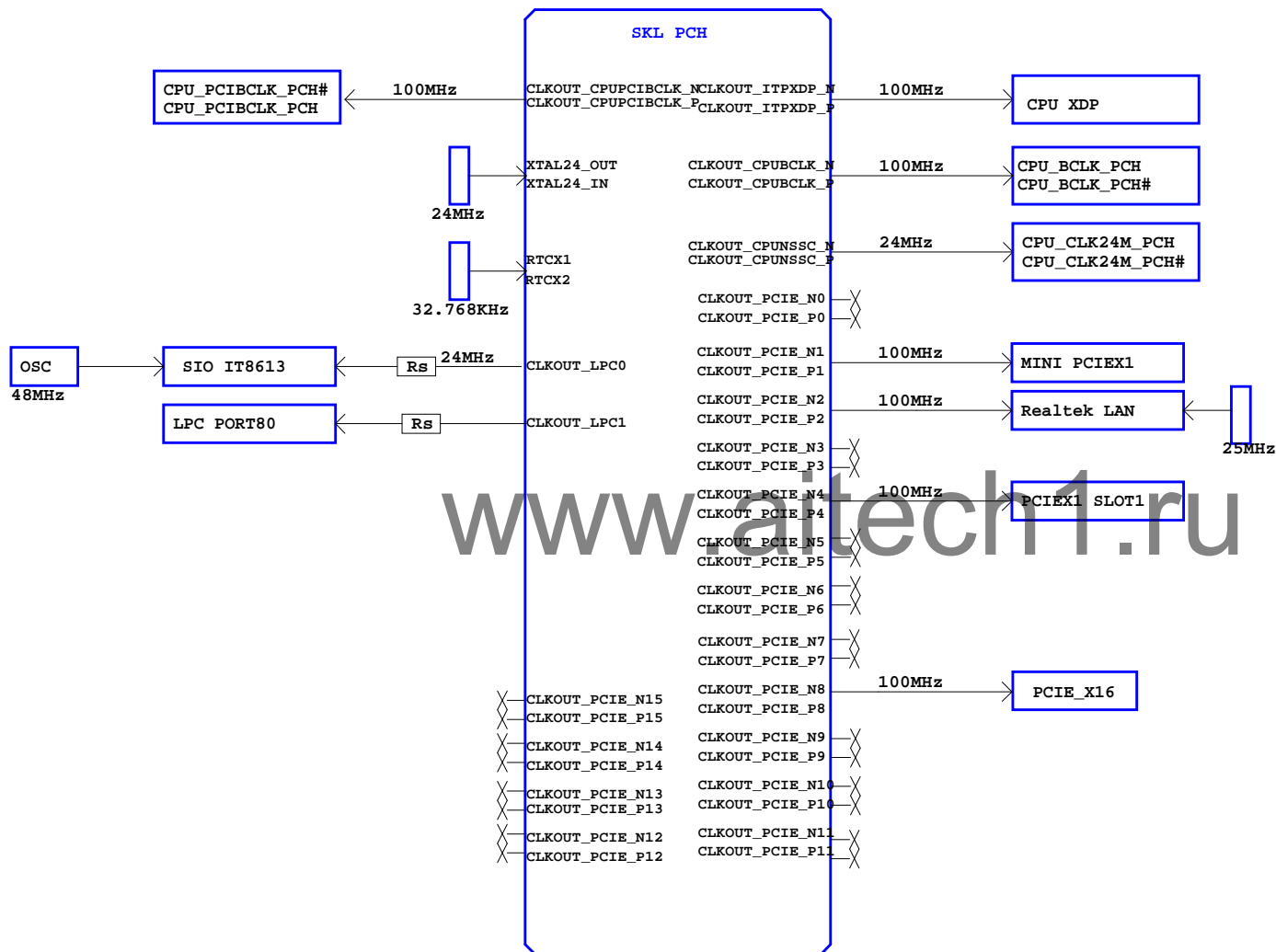


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| Title <b>Change History</b>   |   |   |
| Size<br>C   | Document Number<br><b>Consumer AIO Scotland</b> | Rev<br>SA   |
| Date:   | Friday, August 21, 2015                         | Sheet 107 of 107  |